Digital Equipment Corporation
Maynard, Massachusetts

digital

PDP-8
Maintenance Manual

KV GRAPHIC DISPLAY SYSTEM

DEC-8I-H6MA-D

PDP-8
KV GRAPHIC DISPLAY SYSTEM MAINTENANCE MANUAL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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INTRODUCTION

This publication covers maintenance instructions for the KV Graphic Display System manufactured by the Digital Equipment Corporation, Maynard, Massachusetts. The instructions in this manual are directed to the basic configuration of the system (KV Controller, the VT01 Storage Tube Display, and the H306 Joystick Controller) and its implementation into the PDP-8, 8/I, 8/L, 8/S, 12 and LINC processor.

This manual is intended for use by personnel responsible for installation and maintenance of the KV Graphic System and is arranged into the following seven chapters:

Chapter 1 – briefly describes the system and its general specifications.

Chapter 2 – contains instructions for inspecting, installing, performing preliminary checkout and adjusting the equipment.

Chapter 3 – contains a description of the operating controls and indicators and provides the instruction set, along with sample programs, for programming the system.

Chapter 4 – contains a functional block diagram discussion of the KV controller together with a detailed circuit analysis of each of the individual functional circuits that comprise the basic controller. In addition, a discussion of operational amplifiers and other circuits is provided to aid in the understanding of the operation of the KV controller.

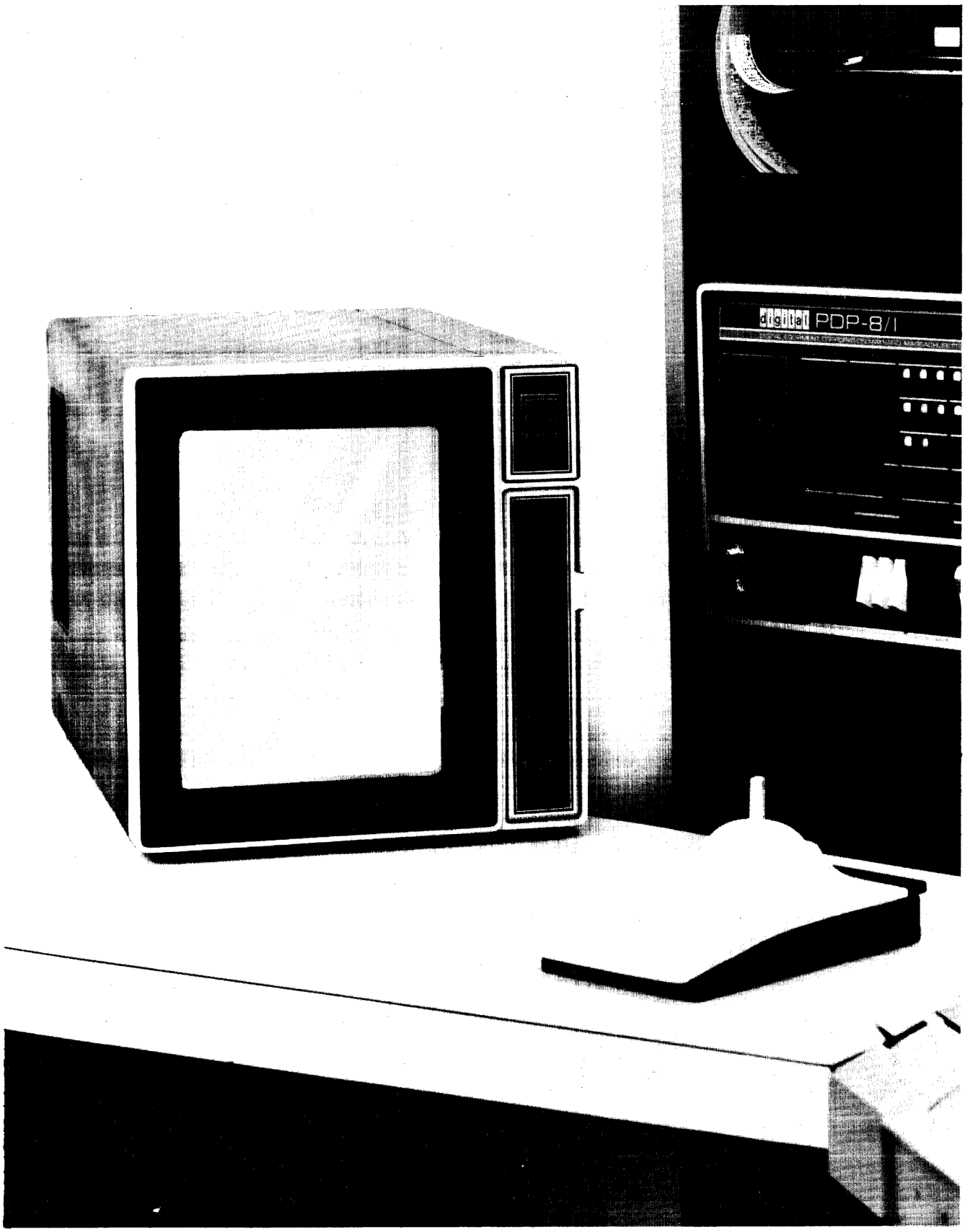
Chapter 5 – contains maintenance instructions for the equipment. Included in this chapter are warranty and service policies of the Digital Equipment Corporation and alignment and adjustment, preventive and corrective maintenance, and repair and replacement instructions.

Chapter 6 – lists and locates each of the replaceable parts of the KV controller to facilitate repair parts procurement for the equipment.

Chapter 7 – contains the necessary engineering drawings to assist in the performance of maintenance tasks.

Related Documents

	Title	Publication No.
PDP-8/I	Maintenance Manual	DEC-8I-HR1A-D DEC-8I-HR2A-D
PDP-8	User's Handbook	
	Maintenance Manual	F-87
PDP-8/L	User's Handbook	C9
PDP-8/S	User's Handbook	F85S
	Maintenance Manual	F-875
PDP-12	User's Handbook	DEC-12-GRZA-D
LINC-8	User's Handbook	F-L85P
	Maintenance Manual	F-L87
VT01	Storage Display Unit Instruction Manual	Type 611, Tektronix (Modified)



Type KV Graphic Display System

CHAPTER 1
GENERAL INFORMATION

1.1 GENERAL

The basic KV Graphic Display System (consisting of the KV controller, the VT01 Storage Tube Display Unit, the optional H306 Joystick Controller, and associated cabling as shown in the frontispiece) may be used with a PDP-8, 8/I, 8/S, 8/L, 12 or LINC computer. The system can be expanded to a multi-terminal (up to eight display units on line) with the addition of the Multiplex Interface Option and VT02 Storage Tube Display Units with keyboards.

1.2 PURPOSE OF THE EQUIPMENT

Common applications of computer graphic display systems permit immediate solution of a broad range of electrical, physical, and mechanical design and analysis problems. While there can be little doubt about the value of the computer in solving complex design problems, the graphic display system accelerates the exchange of data between the user and the computer. Visualization of a problem, whether it be a simple curve that displays the interaction of two variables or a complex network synthesis, permits rapid selection of new parameters. Graphical output permits the user to create a visual model of an electrical, hydraulic, mechanical, or other system while the computer operates on its mathematical counterpart. Thus, parameters that define a point outside a curve can be immediately displayed as irrelevant data, the change in the cross section of a beam can immediately reveal its ability to withstand a given load, and a change in the value of a resistor can immediately demonstrate the relative stability of an electrical circuit.

1.3 BASIC SYSTEM DESCRIPTION

The basic KV Graphic Display System, shown in Figure 1-1, consists of a Type KV Controller, a VT01 Display (Modified Tektronix Type 611 Storage Display Unit), a Type H306 Joystick Control (that permits the user to locate a visual nonstored spot or cursor anywhere on the usable image area of the display), and a Teletype Model 33 Automatic Send-Receive (ASR-33) Keyboard, all working into an 8-family, LINC or PDP-12 Central Processor. Software includes a 64-character (ASCII-compatible) symbol generator, a general-purpose text editor, a graphics interactive programming system called EDGRIN (for EDitor with GRaphic INterpreter), and a cursor reading subroutine that can be used to define the position of the joystick-generated cursor upon command of the user.

1.3.1 KV Controller

The basic KV Controller, shown in Figure 1-1, consists of the four modules: (1) Type A712 Voltage Regulator, (2) Type M712 Timing Generator, (3) Type A612 Digital-to-Analog Converter and Gate Logic Module and (4) Type A312 Analog Function Generator. These modules are described in the subsequent paragraphs.

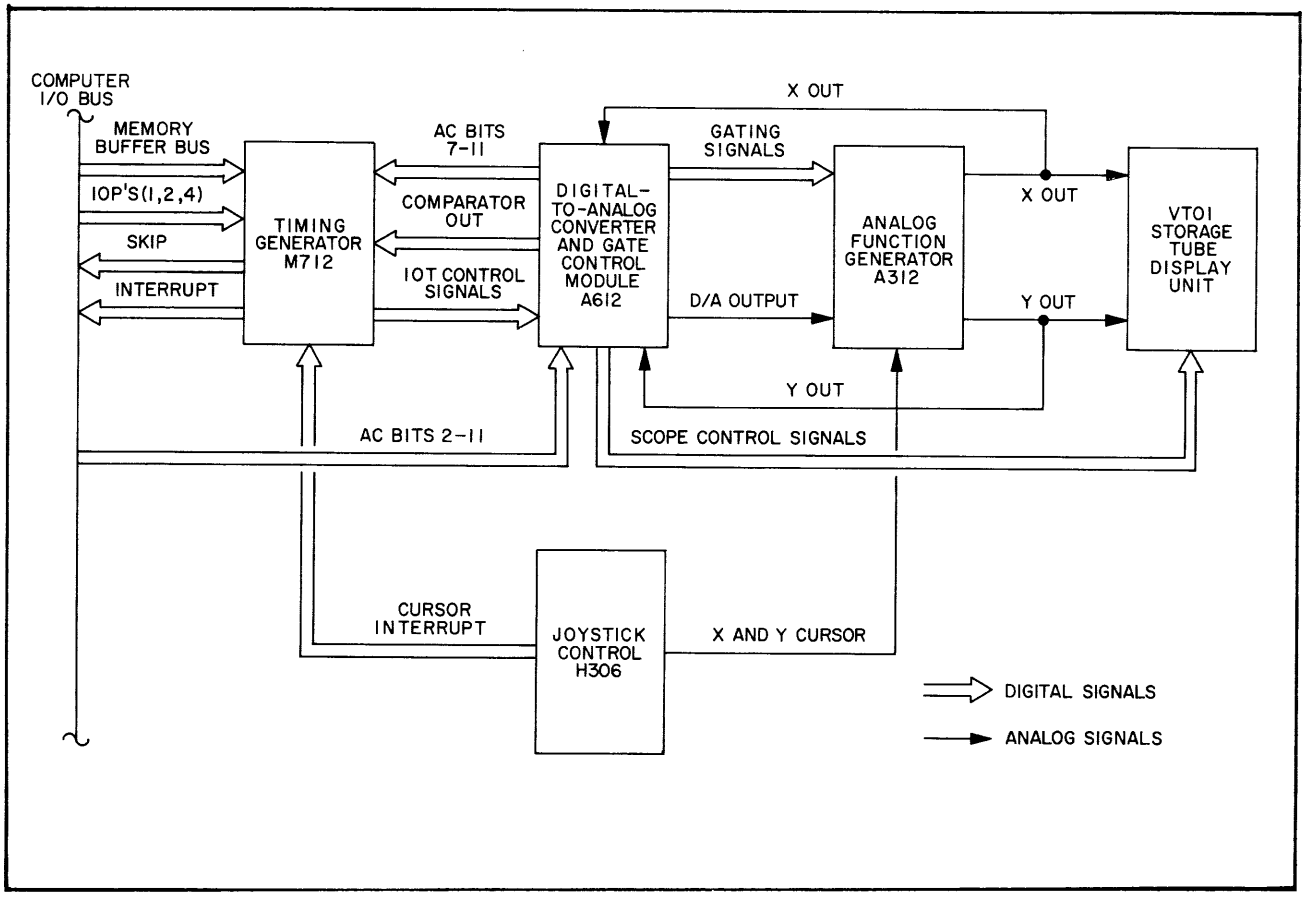


Figure 1-1. KV Controller, Simplified Block Diagram

Type A712 Voltage Regulator Module

The A712 module converts 60-cycle power to regulated ± 11.5 volts which is used by the modules in the controller. Primary a-c power is supplied to the module by a step-down transformer which must be installed onto the CPU main frame. Other dc voltages required by the KV controller are supplied from the CPU.

Type M712 Timing Generator Module

This module decodes the input IOT instructions from the computer and generates system timing signals in synchronism with the computer machine cycle. This module has an internal adjustment that controls vector stroke timing.

Type A612 Digital-to-Analog Converter and Gate Module

This module contains a digital-to-analog converter (D/A) which converts a 10-bit word to a dc analog signal ranging from 0 to -4 volts. Included in the D/A is a comparator which permits program controlled analog-to-digital conversions to locate the position of the joystick in the cursor mode. This module contains four controls for adjustment of the comparator. The module also contains the input data buffer, which receives data-word inputs from the computer, and generates gating signals which are applied to the A312 Analog Function Generator module. These gating signals establish analog signal paths; hence, the mode of operation of the system.

Type A312 Analog Function Generator

The Type A312 Analog Function Generator receives 10 gated outputs and the analog output of the D/A from the Type A612 D/A converter. The gating signals establish the permanent signal paths of the module. The module converts the analog output of the D/A to the appropriate X and Y deflection voltages for the VT01 display. This module contains 22 controls for adjustment of point, vector, and circle patterns on the VT01 display.

1.3.2 Type VT01 Storage Tube Display Unit

The Type VT01 Storage Tube Display Unit (Figure 1-2) is a modified Tektronix Type 611 Storage Display Unit that is driven by the output signals from the KV Controller. The VT01 Storage Display Unit contains a Type T6110 bistable direct view storage tube, which has an aspect ratio of 3/4 and which measures 16 x 21 centimeters (6-1/2 x 8-1/4 inches). The display has a resolution of 400 vertical and 300 horizontal stored line pairs. Two front panel pushbuttons allow the user to select either a VIEW or an ERASE mode.

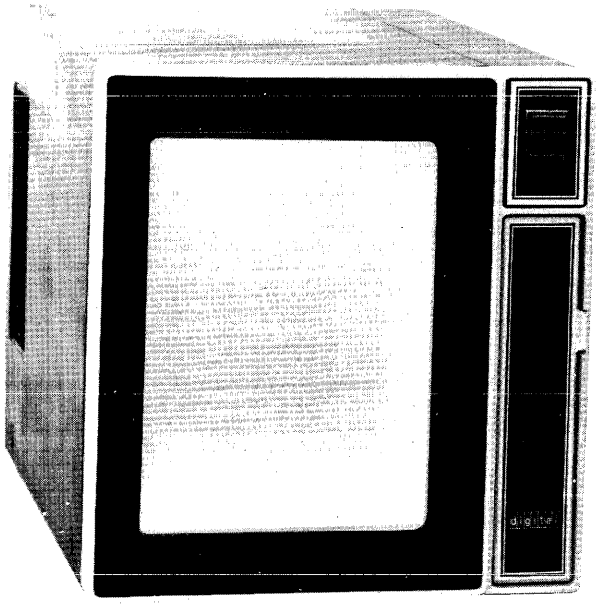


Figure 1-2. Type VT01 Storage Tube Display Unit

An additional mode that is utilized by the KV Controller is the write-through mode. The write-through mode of operation is used to locate and position the cursor with the Type H306 Joystick Controller. When the cursor is moved, the small generated circular spot will not be stored by the display nor will it destroy previously stored information.

1.3.3 The H306 Joystick Controller

The H306 Joystick Controller (Figure 1-3) is the means by which the user can interact directly with the graphical or text information presented by the system. The joystick is used to position the cursor anywhere in the effective image area of the display. The joystick output produces two analog voltages corresponding to the X and Y position coordinates (address) of the cursor. The coordinate addresses are read into the computer, when commanded by the interrupt button. A successive approximation program together with the digital-to-analog circuits of the KV Controller produce a digital representation of the cursor position in the accumulator of the computer.

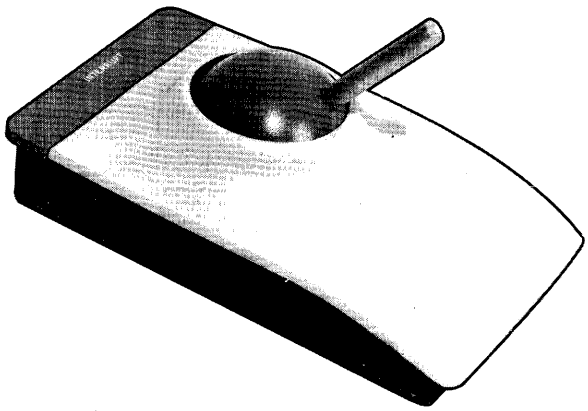


Figure 1-3. Type H306 Joystick Control

1.3.4 Model 33 Automatic Send-Receive Keyboard

The Teletype ASR-33 keyboard (Figure 1-4) is the means by which the user enters the digital data into the computer. The keyboard is the link between the user, the display and the computer. Commands entered into the computer through operation of the keyboard are processed by the computer and stored as data, or perform some manipulation of the viewed display.

1.4 OPTIONS

1.4.1 Multiplex Interface Option

The KV Graphic Display System can also accommodate a multiplex interface option (which consists of an eight-channel multiplexer module and a line driver module) that permits up to eight remote graphic display consoles to be operated in a time share mode through a single KV Controller. The multi-terminal Graphic Display System combines the assemblies of the basic KV Controller and up to eight VT02 graphic terminals.

1.4.2 Type KVGT Graphic Display Unit

The KVGT Graphic Display Unit (Figure 1-5) is a complete remote station consisting of a VT01 and a keyboard which includes the appropriate interface logic. The KVGT, in multi-station systems, is used with the multiplex interface option exclusively.

1.4.3 VS08 Storage Tube Controller Interface

The VS08 Storage Tube Controller Interface provides a location for basic KV Controller modules in a half-rack of logic circuitry together with a suitable power supply and interface modules to permit operation of the KV Graphic System with the PDP-8, PDP-8/S and LINC Computer Systems. The multiplex interface option can be added to the VS08 interface so that up to eight remote KVGT graphic terminals can be on line in a multi-terminal system.

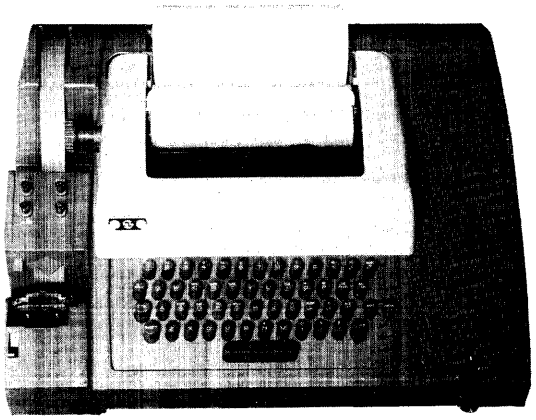


Figure 1-4. Type ASR-33 Teletype Keyboard

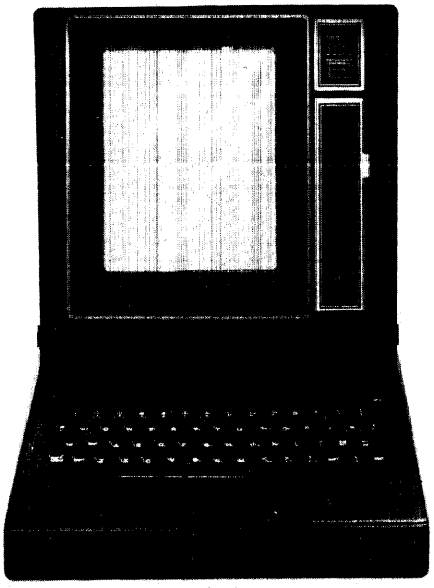


Figure 1-5. Type KVGT Graphic Display Unit

1.5 ACCESSORY EQUIPMENT

Each KV Graphic Display System is shipped with an accessory complement including both hardware and software. The hardware and software complements are described in the subsequent paragraphs.

1.5.1 Hardware

Table 1-1 lists the tools that are supplied with KV Controller. Table 1-2 lists tools that are not supplied, but should be available to properly install and maintain the system.

1.5.2 Software

The type KV software complement is listed in Chapter 7.

1.6 SPECIFICATIONS

The specifications covering the KV Controller are listed in detail in Chapter 7. (Refer to Table 7-1 for page location.)

TABLE 1-1. ACCESSORY HARDWARE COMPLEMENT

Name	Type	Qty	Purpose
Double Module Extender	W983	1	Used to gain access to contacts or components on modules during alignment and maintenance.
Alignment Tool	Bourns	1	Use to access potentiometers for adjustment.

TABLE 1-2. ACCESSORY HARDWARE REQUIRED BUT NOT SUPPLIED

Name	Type	Qty	Purpose
Wrapping Tool	H811	1	Used to wire-wrap terminals of module connectors during maintenance or repair.
Unwrapping Tool	H812	1	Used to unwrap terminals of module connectors during maintenance or repair.

CHAPTER 2
INSTALLATION

2.1 GENERAL

This chapter covers installation of the Type KV Graphics Display System. Instructions are provided for unpacking, transformer installation and wiring, installation of modules and system intercabling. The instructions are based on the assumption that the entire modification and installation will take place at the customer's facility. In cases where this is not true, disregard those instructions that are not applicable.

2.1.1 Power Requirements

Controller – The controller operates from the 115-volt, 60-Hz, single-phase fan power bus of the computer. Internal power supplies provide +11.5 ±1 and -11.5 ±1 volts dc, each at 100 mA. Additional +5 volts at 395 mA and -15 volts at 37 mA are supplied to the controller from the power supplies of the computer.

VT01 – The VT01 operates from a 115-volt, 60-Hz, single-phase source. For 230-volt operation, refer to the Tektronix 611 manual.

Joystick Controller – The Joystick Controller operates from the +11.5- and -11.5-volt power supply of the controller.

2.1.2 Space Requirements

Adequate space should be provided to permit access to the computer and VT01 for maintenance. The outline dimensions of the VT01 are shown in Figure 2-1. (Refer to the applicable computer User's Handbook for computer dimensions.) The equipment should be arranged so that the display unit is clearly visible and the computer console, teletype and Joystick Controller are readily accessible to the operator.

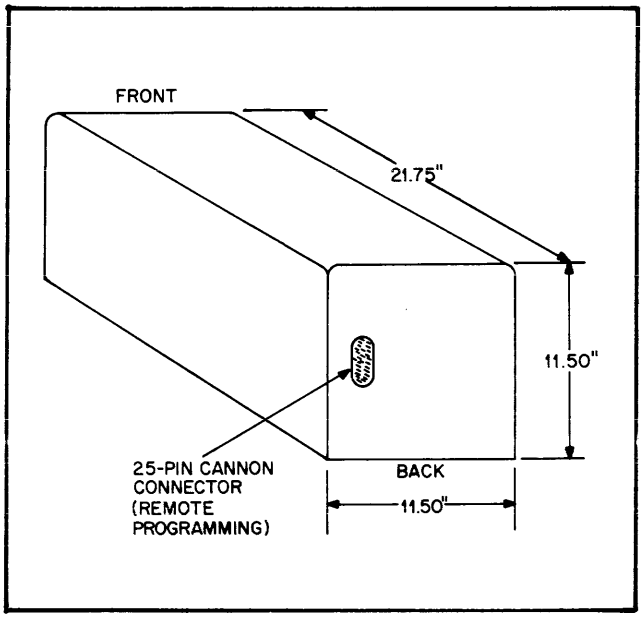


Figure 2-1. Storage Tube Display Unit Overall Dimensions and Location of Remote Programming Connector

2.1.3 Environmental Considerations

The controller operates in an environment ranging in temperature from 10° to 40°C (50° to 104°F) with a maximum temperature deviation of ±3°C (±5°F). The humidity at the installation must not exceed 70%. (Refer to the VT01 instruction manual for environmental considerations for the VT01.)

2.2 UNPACKING

Carefully unpack the equipment and ascertain that the appropriate items have been supplied and that no damage was incurred in shipping.

The following items comprise a typical Type KV Graphics Display System:

1 – Programmed Data Processor and Maintenance Manual

1 – Type VT01 Storage Display Unit and Instruction Manual

1 – Type H306 Joystick Controller (optional)

1 – 20-foot Dual I/O Cable Assembly (Part No. D-IA-7006289-0-0)

1 – Type A712 Power Supply Module

1 – Type M712 Timing Generator Module

1 – Type A612 D/A Converter Module

1 – Type A312 Analog Function Generator Module

1 – Triad F91X Power Transformer

1 – Alignment Tool

1 – Type W983 Module Extender

2.3 MODIFICATION DATA

2.3.1 Computer

The computer modification procedure is applicable to KV Graphics Display Systems that will use a computer that has not been factory wired for the controller. The modification consists of mounting and wiring the Triad 91X step-down power transformer and wiring of the option panel. Perform the following modifications, as required:

NOTE

Refer to Chapter 7 for location of module compartment connectors, associated wiring list and for transformer mounting instructions.

a. Align the transformer mounting holes with the holes in the fan housing and fasten with hardware provided.

b. Connect transformer leads in accordance with the wire list of Table 2-1 using Hand Wire Wrap Tool.

2.3.2 Storage Tube Display Unit

The Storage Tube Display Unit modification alters the write-through and deflection amplifiers to reduce phosphor burnout and noise hazards.

2.4 INSTALLATION AND CHECKOUT

2.4.1 Installation

Install the Type KV Display System as follows:

a. Check the voltage and range selectors at the rear of the VT01 and set them, if necessary, to agree with the line voltage source.

b. Remove the module cover from the PDP-8/I. Check the wiring runs associated with the Triad transformer mounted on the fan housing for physical damage. If no damage is found,

TABLE 2-1. PDP-8/I MODIFICATION WIRING LIST

Wire Color	From	To	Function
Blk/Wht	Fan Pwr AC	Xfmr Primary	AC Input
Blk/Red	Fan Pwr AC	Xfmr Primary	AC Input
Grn	H21N2	Xfmr Secondary	AC Output
Yel	H21F2	Xfmr Secondary	AC Output
Red	H21R2	Xfmr Secondary	AC Output

plug the A712 power supply modules into location H21 and power up the computer. Using a voltmeter or oscilloscope check for +11.5 ±1 volts dc at H21-U2 and -11.5 ±1 volts dc at H21-K2. Turn off the computer.

c. Place VT01 in a convenient location to the CPU and teletype and within the limits of the Dual I/O Cable Assembly. The H306 Joystick Controller is placed beside the VT01 either to the left or right side depending on the operator. Plug the G778 module end of the Dual I/O Cable into location J21 and route the cable to the back of the CPU, teletype and VT01 so as not to interfere with the operator. Plug the cannon connector into the remote program connector located at the rear of the VT01. Plug the 9-pin amphenol connector into the back of the H306 Joystick Controller. This completes the cable connections.

d. Install the remaining modules in their proper compartment locations.

2.4.2 Checkout

VT01 Operating Precautions

To prolong the useful life of the cathode ray tube, observe the following precautions when operating the equipment.

a. Adjust the DRIVE control for the minimum writing gun-beam current level that will produce a clear, well-defined display. Excessive beam current may cause either a bright burn condition or, if intense enough, a more serious dark burn condition. A bright burn condition is the appearance of a residual display image after erasure. Bright burn images can be erased by adjusting the OPERATING LEVEL control to establish a fade-positive condition. The time required for a fade-positive condition to effect a complete erasure is dependent on the severity of the burn. A severe burn may require up to 12 hours for complete erasure. Operate the instrument in the fade-positive mode only as long as necessary, since in addition to the loss of useful operating time, extended fade-positive operation will decrease the life expectancy of the CRT. A dark burn condition is the destruction of the cathode ray tube phosophor by the intensive beam current. This condition is evidenced by a spot or area that will not react to the writing gun. As with a conventional CRT, the only remedy for this condition is replacement of the cathode ray tube.

b. Erase the display when the information is no longer needed. If a display is left on the CRT for an extended period of time, it can cause a residual image that may appear as a negative image of the erased display or a positive image superimposed on the new display. Whether the image appears positive or negative will depend on the brightness level of the image phosphor as compared to the brightness level of the new display's background phosphor. The residual image may be erased by establishing a fade-positive condition.

VT01 Set-Up

This procedure positions the front panel controls prior to the application of power.

Preliminary Instructions

a. Disconnect all external signal cables from the rear panel connectors.

b. Set the front panel controls as follows:

POWER	OFF
WRITING INTENSITY	CCW
OPERATING LEVEL	Do not change the setting of this control.
FOCUS	Midrange
TEST SPIRAL	NORMAL

c. Ensure that the rear panel VOLTAGE and RANGE selectors are set to the appropriate positions for the available power source and then connect the power cord to the power source.

VT01 Energizing Procedure

a. Turn the POWER switch to ON. The ERASE switch should illuminate and as the instrument warms up, the display area of the CRT should assume the bright luminance of a fade-positive condition.

b. Press and release the ERASE switch. The instrument should cycle through an erase function and assume a ready-to-write condition. The display should appear to be at a uniform luminance level, much lower than the brightness level of the fade-positive condition.

c. Slowly turn the WRITING INTENSITY control in a clockwise direction while observing the display for the indication of a bright spot. If a bright spot appears, immediately turn the control counterclockwise. If the control can be turned fully clockwise without a spot appearing, this test of the instrument operating condition is normal. Set the WRITING INTENSITY control to midrange and proceed.

NOTE

Storage capability and resolution are affected by the interaction of the OPERATING LEVEL, WRITING INTENSITY and FOCUS control settings.

d. The OPERATING LEVEL control provides adjustment of the Storage Target Backplate potential. The procedure for this adjustment is given in Chapter 3 of the Tektronix Manual.

e. Pull the TEST SPIRAL switch to its FOCUS position. A spiral waveform should appear on the display. Adjust the FOCUS and WRITING INTENSITY controls for an overall clear, well-defined display of the desired viewing brightness.

f. Push and hold the TEST SPIRAL switch to its spring-loaded STORE position for about 3 seconds or until a stored spiral waveform appears on the display. The stored spiral should remain clearly visible for about 60 to 90 seconds, then appear to be almost erased as the VIEW switch is illuminated. An illuminated VIEW switch indicates that the instrument is in a holding mode of operation.

g. Press and release the illuminated VIEW switch. The stored spiral should again appear on the display and the VIEW switch should be extinguished. The instrument should remain in this condition for about 60 to 90 seconds and again assume a holding mode of operation.

h. Press and release the ERASE switch. The instrument should cycle through an erase function and assume a ready-to-write condition. This completes the instrument-energizing procedure.

Type KV Graphics Display System Checkout

Refer to Chapter 5 and load and run the MainDEC diagnostic self test routines. Perform the alignment and adjustment procedure contained in Chapter 5 to the extent required to align the system.

CHAPTER 3
OPERATION AND PROGRAMMING

This chapter is divided into two sections which provide operation and programming instructions for the Graphic Display System described in this manual. With the exception of oscilloscope adjustments and joystick manipulation, there are no special operating procedures described in Section I. The techniques for programming described in Section II are at the machine-language level. Source level programs are generated using EDGRIN, a special source-language assembler that simplifies the work of originating a graphic display. EDGRIN commands deal almost exclusively with input-output program modifications, line and text display, compilation and execution of programs written in the EDGRIN language. This language gives EDGRIN the properties of an editor, compiler and operating system.

SECTION I
OPERATION

3.1 GENERAL

With the exception of some VT01 Display adjustments, required prior to operation, and the MAINDEC diagnostic routines, described in Chapter 5, there are no special operating procedures for the graphic display system. Operation of the VT01 Display and the H306 Joystick Cursor Control (with the exception of manually selected coordinate positions and a program interrupt), is determined entirely by the KV Controller and the source program. However, during maintenance checkout, certain controls on the computer console and certain adjustments at the KV Controller modules must be made. Switches and controls on the VT01 Display are shown in Figure 3-1.

3.2 OPERATING CONTROLS

Visible on the VT01 Display front panel are two pushbuttons; below these pushbuttons is a panel door which, when opened, exposes the power switch and five vernier controls. The functions of these controls are described in Table 3-1.

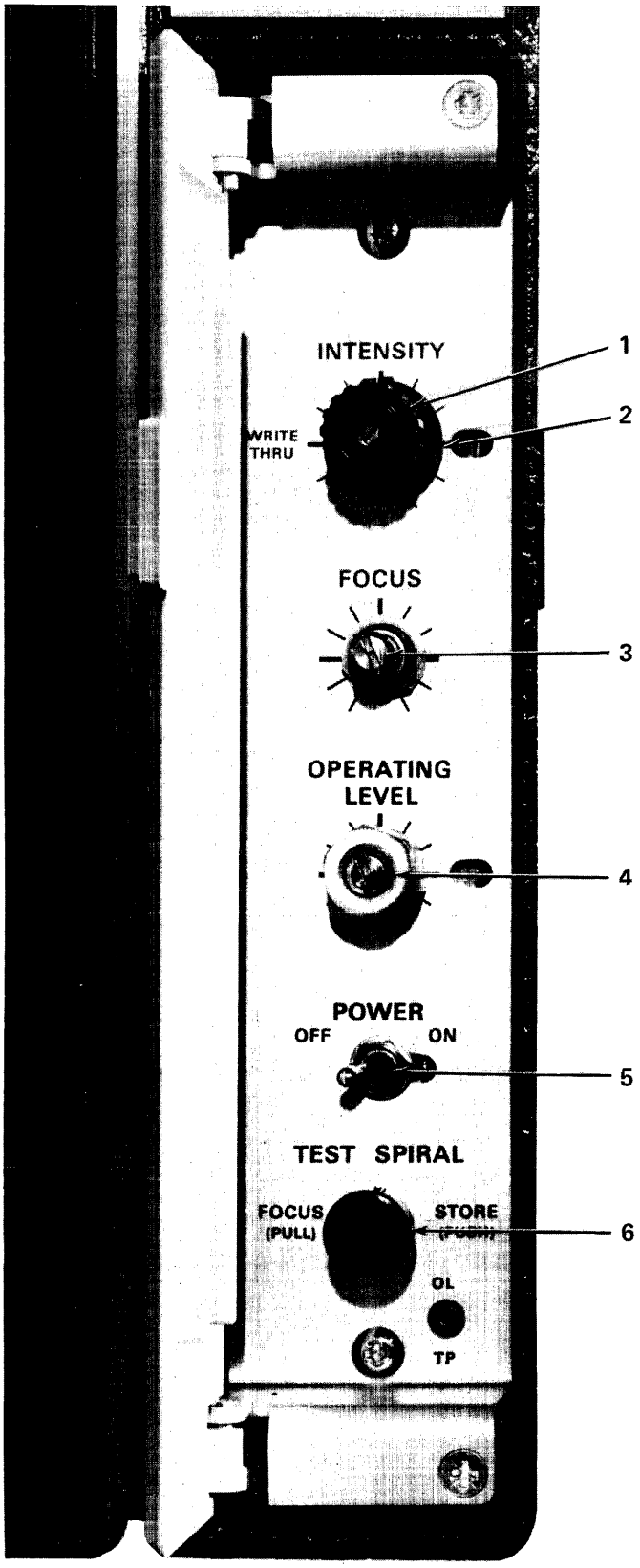


Figure 3-1. Storage Tube Display Unit VT01, Location of Controls and Indicators

TABLE 3-1. FUNCTION OF CONTROLS AND INDICATORS, GRAPHIC DISPLAY SYSTEM

Index No	Name	Function
Not Shown	ERASE pushbutton	Used to delete all stored information from the storage tube (oscilloscope). NOTE The VT01 display has a hardware safety feature that controls the intensity of the display. When an image has been displayed for 90 seconds, and no additional information has been added to the display, this device reduces the intensity of the display. Thus, the display appears to vanish; however, this reduction in the intensity of the display has no effect on the information stored on the oscilloscope image area.
Not Shown	VIEW pushbutton	Used to restore the display to full intensity for a new 90-second period.
1	INTENSITY control (outer concentric)	Used to adjust the intensity of the writing beam during normal writing functions.
2	Write-Thru INTENSITY control (inner concentric)	Used to adjust the intensity of the writing beam during write-thru writing functions.
3	FOCUS control	Used to obtain a sharply defined writing beam. This switch is used in conjunction with the TEST SPIRAL pushbutton (6).
4	OPERATING LEVEL control	Used to adjust the storage properties of the oscilloscope. This control, adjusted during installation, does not normally require a change in setting.
5	POWER switch	Used to energize the Storage Display Unit.
6	TEST SPIRAL pushbutton	Used to change the oscilloscope circuits from a normal operating configuration to either of two test configurations. The test positions are Store and Focus.

TABLE 3-1. FUNCTION OF CONTROLS AND INDICATORS, GRAPHIC DISPLAY SYSTEM (cont)

Index No.	Name	Function
6 (cont)	Normal	When the TEST SPIRAL pushbutton is in its center position, the oscilloscope circuits are configured for normal operation.
	Store test	When the TEST SPIRAL pushbutton is depressed and held in for one second or longer, a stored spiral waveform should appear on the oscilloscope. This spiral waveform should remain intensified for between 60 and 90 seconds whereupon the VIEW switch will light and the displayed image will appear to be erased. When the VIEW switch is illuminated, the oscilloscope will enter its store mode. Depressing the VIEW switch again will restore the spiral image.
	Focus test	When the TEST SPIRAL switch is pulled out to its focus test position, a spiral waveform should appear on the oscilloscope. The FOCUS control should then be adjusted for the sharpest image on the display.
Not Shown	TYPE H306 JOYSTICK CONTROLLER INT pushbutton	When depressed, a software routine automatically places the digital equivalent of the coordinate value of the cursor position in the PDP-8/I accumulator.
Not Shown	Joystick control	This control can be moved in two axes. Its position defines the position of a spot, called a cursor, on the image area of the oscilloscope.

SECTION II
PROGRAMMING

3.3 GENERAL

The descriptions in this section are addressed to machine-language programming requirements and acquaint maintenance personnel with the controller instruction-word set. Parameter and data-word formats are described so that simple machine-language programs can be compiled for the purpose of testing and checkout of the KV Graphic Display System. Also, simple display routines are given as samples.

3.4 DISPLAY CAPABILITIES

The KV Graphic Display System, which comprises the controller and the VT01 display, has four primary line-drawing capabilities and a

software-controlled text generation capability. The four graphic constructions are:

a. Straight Lines
b. Points
c. Circles
d. Arcs

3.5 THE OSCILLOSCOPE DISPLAY

The oscilloscope display (or image) area (Figure 3-2) is divided into a square four-quadrant rectangular coordinate system whose effective area limits are ± 512 decimal (1000 octal) units along both the X and Y axes (this is approximately 85 decimal (125 octal) units/linear inch). Of this effective area, the visible image-area limit along the X-axis is ± 256 decimal (0400 octal) units; along the Y-axis the visible limit is ± 320 decimal (0500 octal) units.

3.5.1 The Addressable Coordinates

All coordinates are expressed either in terms of their displacement from the origin or with respect to the last program-named coordinate position. Any point within the image area must be defined by both its X-axis and Y-axis coordinates with the X-axis coordinate always expressed first. If the desired position of a coordinate is given as absolute, its displacement is taken from the origin. If the desired coordinate position for either axis is expressed as relative, its displacement is taken from the last named position for that axis.

In machine-language programming the characteristics of the desired graphic form, such as point, line, arc, or circle, must be specified together with the X- and Y-axis coordinates that locate the position of the line form in the display. These requirements are met by two distinct word formats that are used to define the characteristics and the coordinates; the parameter word defines the desired line form characteristics and the data word locates the X- and Y-position coordinates of the line form. In this description, both parameter and data words are expressed as octal numbers, but are written into the accumulator or memory registers of the computer and the registers of the controller, as binary numbers. When using EDGRIN as the source language, the parameter words are predetermined through programmer selected ASCII characters by the EDGRIN assembler. The X-axis and Y-axis coordinates, however, are expressed as digital numbers by the programmer but assembled as binary numbers by EDGRIN.

3.5.2 Visible Image Area

The visible image area of the display oscilloscope is normally used when defining a coordinate position. Any definable point in the visible image area is considered as the hardware limit. Any definable point between the visible image area and the effective image area (shaded area, Figure 3-2) is considered a software limit. All addressable coordinates should lie within the visible image area unless origin shifting, scaling, or light button features of EDGRIN are used. Origin shifting, scaling, and light button features of programming are described in the EDGRIN Programming Manual and are beyond the scope of this publication.

3.5.3 Line-Drawing Capabilities

The KV controller draws lines on the oscilloscope screen through a linear vector stroke that is generated by the controller analog function generator module. Depending on whether the

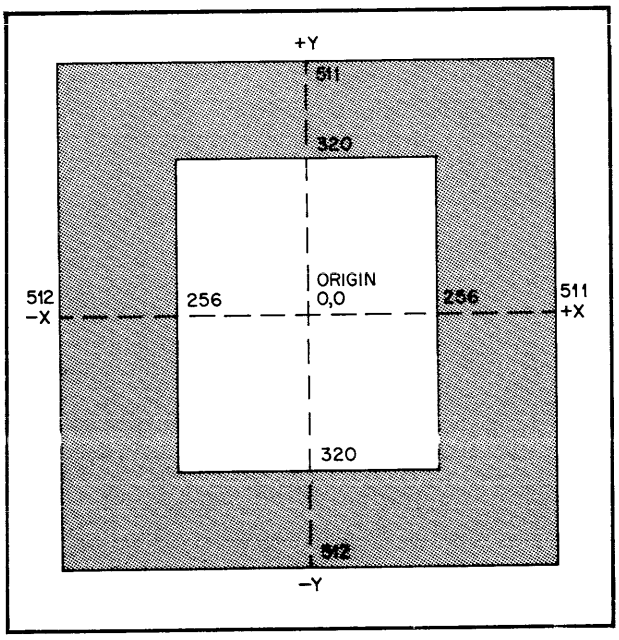


Figure 3-2. Effective and Visible Image Areas

starting and end-point coordinates for the linear stroke to be generated are referenced to the origin or to the last named coordinate positions, the stroke generation format is expressed as absolute, or relative, respectively.

Linear Vectors

Parameters that define a wanted linear vector are short or long, relative or absolute, and intensified (visible) or unintensified (invisible). Such linear vectors are always drawn between a given coordinate location and an end point which can be specified in either absolute or relative mode and are executed in either a short or long format. The vector can be drawn visible or invisibly between the given starting point and specified end point.

The end-point coordinates may be specified relative to the given starting point coordinates by specifying the relative mode and sequentially entering the X and Y coordinate positions, which define the incremental displacement (ΔX and ΔY) of the line along the X- and Y-axes (Figure 3-3), into the X and Y sample and hold registers (XSH and YSH, respectively) of the controller. The end-point coordinates may also be entered absolutely (with respect to the origin) by specifying the absolute mode and sequentially entering the coordinate positions, which define the absolute displacement of the end point along the X- and Y-axes, into the X and Y sample and hold registers, XSH and YSH, of the controller.

Drawing Modes – Relative and absolute modes are program ordered by depositing the desired parameter as a binary bit of a 9-bit parameter word into the PDP-8 family accumulator and then issuing an execute input-output transfer instruction. Other line-vector parameters that are defined by the 9-bit parameter word are long and short format, the intensification of the wanted line, erasure of the display currently shown on the oscilloscope screen, and integrator reset. An integrator reset ensures that the line-vector will be properly referenced to the origin. If the integrator reset is not specified by one of the bits in the parameter word, the line vector should start from the last named end point.

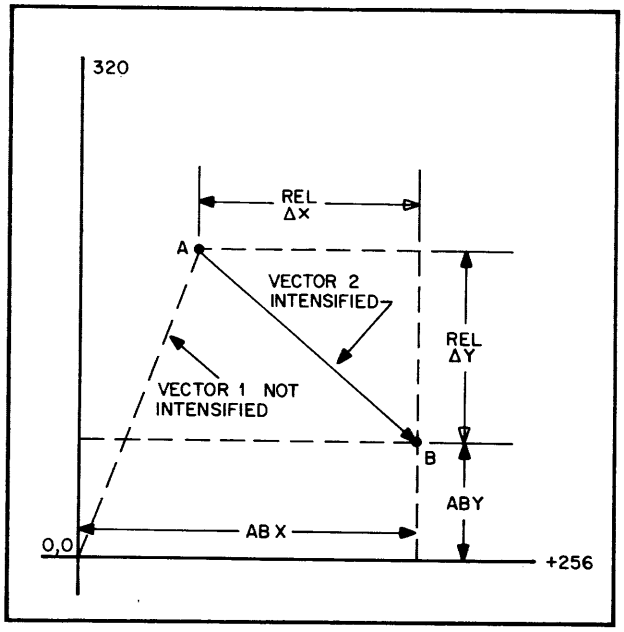


Figure 3-3. Specification of Start and End Linear Vectors

Figure 3-3 shows two linear vectors: vector 1, which is illustrated as the dashed line, has its starting point at the origin and is drawn unintensified (invisibly). The coordinates of end-point A of vector 1 are (85,255). This vector can be expressed in relative mode if the integrator reset bit in the parameter word was previously set, or directly in absolute mode. The coordinates of end-point B of vector 2 are 255,85 absolute or 170, 170 relative. This vector would be specified as long because it is greater than 3/8 inch in length and should be drawn intensified so that it will be displayed on the oscilloscope image area.

Long and Short Linear Vectors – The length of the generated linear vector stroke is determined by the stroke-control timing circuits in the controller. For line vectors, the stroke-control timer operates at two discrete time intervals depending upon whether a long- or short-stroke bit is set in the 9-bit parameter word. When a long stroke is chosen, the stroke control timer will provide a time signal 2700 machine cycles long (for a total of 4.05 milliseconds at 1.5 microsecond/machine cycle). When a short stroke is chosen, the stroke control timer will provide a time signal that is 1/16 the period of the long stroke time period (for a total of 250 microseconds). The vectors illustrated in Figure 3-3 are long.

Long Linear Vectors

A long vector execution is required if the vector length exceeds 3/8 inch. Choosing the long-vector bit in the 9-bit parameter control word for a line less than 3/8 inch in length will cause deterioration of the line quality which will result in excess line width and low resolution.

Whenever the vector length is over 3/8 inch but less than 6 inches, the long vector bit should be specified in the parameter word. When the starting X- and Y-axis coordinates for the vector are chosen, and if these coordinates do not occur at the origin in the display, an invisible vector must first be drawn to the starting point of the visible vector. The visible vector A•B in Figure 3-3 is drawn in just this manner. The programming sequence is as follows:

a. The oscilloscope display is first erased and the integrators in the controller are reset to obtain an origin (0, 0) starting-point setting both the X and Y integrators.

b. Next the X-axis coordinate is loaded into the X-axis sample and hold register and the Y-axis coordinate is loaded into the Y-axis sample and hold register. This occurs as two sequential subroutines in the program.

c. The parameters for the vector are then loaded into the computer accumulator in their proper bit positions and an absolute long nonintensified vector is executed. When the output voltage from the integrators equals the same voltage level as that of the analog value of the end-point (A) coordinates in the respective sample and hold registers, an invisible vector will have been executed to point A.

d. When the vector is executed, the program is held in a waiting-loop microprogram called a skip test, until the vector is completed. At the completion of the vector, the controller returns a skip signal (ready flag) to the interfacing computer to permit the program to continue.

e. To generate the visible vector A•B the X-axis coordinate of point B is loaded into the X-axis sample and hold register and the Y-axis coordinate of point B is loaded into the Y-axis sample and hold register.

f. The parameters for the visible vector are then entered into the accumulator of the computer in their proper bit positions so that an absolute (or relative, depending on how the X- and Y-axis coordinates were chosen) long intensified vector is generated. The execution of this vector causes the output voltage of the respective X and Y integrators to be driven to the same analog levels as those held in the respective X and Y sample and hold registers.

g. The program is held in the skip test waiting loop until the ready flag is detected. This completes the execution of the visible vector A•B.

NOTE

Unlike digital registers a property of analog registers is their inability to remember their values over long periods of time. Thus, all analog registers are subject to drift. In the KV Controller this drift is not greater than 30 spot positions per second in the sample and hold registers and 6 spot positions per second for the integrate and hold registers, over a ± 3° C (± 5° F) range about the ambient temperature when they are initially adjusted. This spec means that some care must be taken to reset the integrators when analog data is not renewed. Hence, it is a good practice to reset whenever a vector sequence is broken.

Short Linear Vectors

A short vector execution is desired if the vector length is less than 3/8 inch. Choosing the short vector bit in the 9-bit parameter control word, for a line greater than 3/8 inch in length, may exceed the storage capability of the oscilloscope and the accuracy of the KV-8 Controller.

3.5.4 Circle-Drawing Capabilities

The KV-8 controller is capable of drawing arcs and circles on the oscilloscope with a circular vector stroke that is generated by the controller analog function generator module. An arc or circle is drawn by first specifying the X- and Y-coordinates of a point on the circumference of the wanted circle and then initializing the integrators to these values using the linear vector mode and drawing an invisible linear vector to this point. This point defines the start of the arc or circle vector. Next, the X- and Y-coordinates of the center of the circle are determined relative to the origin at 0,0 and then the arc or circle is drawn in circular vector mode using the coordinates of the center. Depending on the length of the arc, it may be executed in either short, long, or continuous circular vector mode. The difference between the center coordinates and the circumference coordinates determines the radius of the circle or arc.

Circular Vectors

Parameters that define a wanted circular vector are short, long, or continuous; and intensified or unintensified. Circular vectors are always drawn clockwise with respect to the starting location. The arc or circle can be drawn visibly or invisibly between a given starting point and the end point. The starting point coordinates must be specified first; then the center of the arc or circle is computed to give the radius. In Figure 3-4, the circular vector is specified by giving the X and Y coordinates of starting point A as absolute from the origin. A linear vector is then drawn invisibly to point A to give the start of the wanted arc. Next, the coordinates of point B are specified and the circular vector is drawn. (The coordinates for the center of a circle in circular arc mode are always referenced to the origin 0,0.) If a short vector has been chosen, the arc will subtend 5.625°; if a long vector has been chosen, the arc will subtend 90°; and if a continuous vector has been chosen, the arc will be continuously drawn until the arc is stopped by giving the suitable stop command.

Long and Short Circular Vectors – The arc angle of a generated circular vector stroke is determined by the stroke-control timing circuits in KV controller. For arc vectors the stroke-control timer operates at two discrete intervals depending upon whether a long or short circular stroke bit is set in the 9-bit parameter word. When a long stroke is chosen, the stroke control timer will provide a time signal that permits an arc of 90 degrees to be subtended. The circular vector illustrated in Figure 3-4 is long.

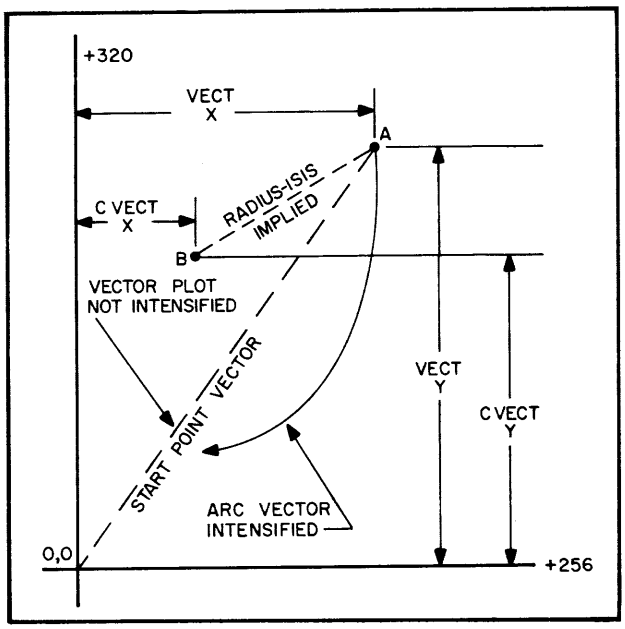


Figure 3-4. Specification of Center, Start and Circumference of Circular Vectors

Whenever the circular vector to be generated subtends an integer multiple of 5.625°, the short vector mode bit should be specified in the parameter word. The desired arc angle is then obtained by executing the correct number of short circular arc vector commands. When this is done, it may not be necessary to reload the coordinates of the center prior to each execution if the arc can be completed in less than 20 milliseconds (that is, if there is no long wait between the completion of each 5.625° segment and the initialization of the next 5.625° segment).

Continuous Circular Vectors – When a circular arc with an arc angle not divisible by 90° or 5.625° is to be generated, it is necessary that the bit controlling the continuous mode of the 9-bit parameter word be set. Setting this bit disables the vector stroke timer in the controller. Hence,

timing must be controlled externally by the program in a real-time mode. The arc writing rate is 0.1 degree per 4.5 microsecond. Continuous mode may also be used for angles divisible by 90° or 5.625° if desired.

To draw the circular arc shown in Figure 3-4, the following programming sequence is required:

a. The oscilloscope display is first erased and the integrators in the controller are reset to obtain an origin (0, 0) setting in the X and Y integrators.

b. Using the load format to obtain the absolute vector mode, the X-axis coordinate of the linear vector is loaded into the X-axis sample and hold register and the Y-axis coordinate is loaded into the Y-axis sample and hold register. The loading of these registers occurs as two small sequential subroutines in the program:

c. The required parameters are then loaded into the computer accumulator in their proper bit positions and the absolute long nonintensified linear vector is executed. When the output voltage from the integrators equals the same voltage level as that of the analog value of the end-point (A) in the respective sample and hold registers, an invisible vector will be executed to point A.

d. When the linear vector is executed the program is held in the skip-test waiting-loop until the vector is completed. At the completion of the vector, the controller returns a skip signal (ready flag) to the interfacing computer to permit the program to continue.

e. Then, to generate the visible circular vector, the circular vector load format is chosen and the X-axis coordinate of point B is loaded into the X-axis sample and hold register and the Y-axis coordinate of point B is loaded into the Y-axis sample and hold register as in (b) above.

f. The parameters for the visible circular vector are then entered into the accumulator of the computer in their proper bit positions so that a long intensified arc vector is generated. The execution of this vector causes the output voltage of the X and Y integrators to be driven by quadrature sinusoidal signals in such a manner that they trace out the parametric path of a circular arc on the face of the display.

g. The program is held in the skip-test waiting loop until the ready flag is detected. This completes the execution of the visible arc vector.

NOTE

Whenever a circular vector is executed, bit 3 of the parameter word must be set to zero. The parameters for the wanted vector should always be loaded into the accumulator before the execute command is given. Refer to sample programs at end of chapter.

3.5.5 Point-Plotting Capabilities

The KV controller plots points on the oscilloscope screen simply by reading the data-word analog value stored in the sample and hold registers. When a point-plot graph is to be generated it is only necessary to specify the X and Y coordinates of each wanted point in point mode. Spot diameter is 0.008 inch approximately and the distance between addressable screen coordinates is approximately 0.012 inch so that specifying X and Y coordinates in continuous increments of 1 will generate what will appear essentially as a continuous graph of the function of two variables. For points more widely separated, or for estimates of a general direction of the variables, the vector mode should be used to connect the separated points. A short vector (3/8 inch in length) will contain approximately 32 decimal (40 octal) coordinates.

3.5.6 Joystick And Cursor

Any coordinate on the display viewing area can be identified with the Type H306 Joystick Control which slews a small light spot (cursor) anywhere in the visible viewing area in both the X and Y planes. The Joystick control moves in two planes and its physical position corresponds

with the position of the cursor in the viewing area. An interrupt button on the Joystick behind the control permits the computer program to be interrupted on demand from the user. When the program is interrupted, and if the computer is programmed to recognize the interrupt, a routine is entered that obtains the coordinate of the current position of the cursor. The routine must be executed twice, once for each coordinate. (Refer to ADCONV Program Example at end of chapter.)

3.6 BASIC MACHINE-LANGUAGE PROGRAMMING

All parameter-word and data-word transfers between the PDP family computer and the VT01 graphic display take place through the accumulator. Hence, each accumulator-held word must be transferred to the digital register in the controller through an input-output transfer (IOT) instruction. These input-output transfer (IOT) instructions tell the controller whether the word held in the accumulator is a parameter or data word and also what action should be taken by the controller in processing the parameter or data word.

3.6.1 The KV Controller

The KV Controller (Figure 1-1) converts digital data inputs from the computer accumulator into an analog signal that drives the X- and Y-axis deflection circuits of the VT01 Storage Display Unit. The digital inputs required by the Type KV Controller are entered into the accumulator through the computer program stored in its memory, which tells the control what to do with the accumulator data. The program contains data files for generation of any desired ASCII (teletype compatible) character, character string, or any arbitrary vector sequences and an interruptable entry for converting the cursor position coordinates to digital data that immediately updates the data file. The VT01 Storage Display Unit is an unrefreshed system; hence, a large data file or refresh memory is not required to regenerate the display. The oscilloscope itself has a memory so that the amount of computer core storage required for a given display is significantly reduced. The unrefreshed system also permits display data file subroutines and data-file linking programs to be stored in highly compacted algorithms that can be linked in any combination to draw the picture of a desired graphical structure. Once the file subroutines have been programmed, they need only be linked by a main program. These links can be updated by defining new positions with the cursor.

The KV Controller consists of essentially three functional groups: (1) the control and timing circuits, (2) the digital-to-analog conversion circuits, and, (3) the analog function generator. The control and timing section accepts commands from the computer accumulator via the input-output bus, and transmits commands back to the computer through its skip and interrupt facilities in the control logic. The circuits also establish system timing.

The digital-to-analog converter (DAC) produces an analog output that is proportional to the digital number in the accumulator. The number in the accumulator is given in 2's complement notation in bit positions AC_2 through AC_{11} for a total of 10 bits; this 10-bit binary number gives a signed 512 point address range. The third major functional unit is the analog function generator which is actually a hybrid computer. Digital commands to this unit establish various analog functions such as line and vector generation and circle generation.

In programming the KV Controller, instructions are given by a combination of the input-output instruction set and the contents of the accumulator. The KV Controller has two major control states, data and parameter, which are selected by the input-output (IOT) instructions. In the data state, the content of the accumulator is interpreted as a data word representing a positional coordinate (i.e., part of an address) that defines a point on the VT01 display. This position is specified by the IOT instruction which is interpreted as an X or a Y address. This address is accepted by the controller as either an absolute address (which is always referenced to the origin position) or as a relative address (which is always referenced to the previously stored display address).

The interpretation of the address as absolute or relative is determined during the second major state. During this state, called the *parameter state*, the contents of the accumulator are interpreted as a microprogrammed instruction that controls the execution of the desired vector (i.e., long linear vector, short linear vector, circle vector, circular arc vector, or point) within the analog function generator. The parameter control state is also used to control the output display mode of the VT01 display.

The KV Controller uses two independent events to communicate with the computer. The first event is the ready-to-receive event. Whenever an instruction is presented to the control unit in the correct format, the ready flag will be lowered and will then automatically be raised after the instruction has been executed. The ready flag produces an interrupt request which appears on the computer interrupt bus. The status of the ready flag can be sampled by a skip instruction.

The second event that also causes an interrupt is an external interrupt request key physically located on the rear of the joystick cursor control device. When this key is depressed, the status of the cursor flag is sampled by a skip instruction.

In addition to the above two flag skip instructions, a third (non-flag) skip instruction is available; this instruction produces a skip pulse on the computer skip bus if the output voltage of the DAC is greater than the output voltage of the selected cursor axis. This instruction is used to read the X- and Y-axis cursor coordinates through a successive approximation program.

3.6.2 IOT Instruction Format

The IOT instruction is a standard 12-bit word used by the 8 family of computers to elicit specific responses from the peripheral device (the VT01 controller). This 12-bit word (Figure 3-5) comprises three basic multi-bit parts: the computer operation code, the device selection code, and the device operation code.

Computer Operation Code

The computer operation code uses the first three bits of the instruction word; hence, bits 0, 1, and 2 tell the computer that the instruction is an input/output transfer. In the 8 family of computers, this three-bit word is 110 (or 6 octal).

Device Selection Code

The next six bits (3, 4, 5, 6, 7, and 8) of the IOT instruction word are the device selection code. The six-bit length of this code permits up to 64 peripheral addresses. However, many peripheral devices require two or more codes because they can perform a large number of discrete operations. For example, there are three device codes for the KV controller: these device codes are $000\ 101_2$, $000\ 110_2$, and $000\ 111_2$ (05, 06, and 07 octal). Generally device code 05_8 is used with the joystick to recognize or clear the cursor flag; device code 06_8 is generally used to load the X and Y registers of the controller and to execute a wanted vector; device code 07_8 is used to recognize the completion flag and for operation of the digital-to-analog converter and comparator.

Controller Operation Codes

The last three bits (9, 10, and 11) of the IOT instruction are the device operation code. Setting any one of these three bits separately or in combination obtains a wanted response from the controller or from the display. These bits control a timing generator in the computer that provides serial output pulses on the input/output (I/O) bus which are used by the controller to perform its operations. For each of the (7) possible combinations of the output pulses, a separate response is provided by the controller (VT01), but not simultaneously. Although the effective number of separate responses available with the three-bit device operation code is 7, this number is somewhat idealized. In the three-number device selection code group, there are 11 separate operating codes, two in the 05_8 group, five in the 06_8 group, and four in the 07_8 group. The instruction set for the KV controller is listed in Table 3-2.

3.6.3 Programming Techniques

Typical machine-language programs to produce line, arc, and circle generation include the octal

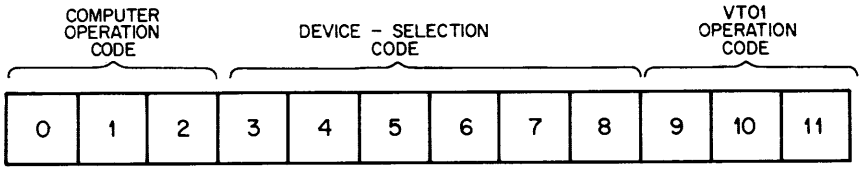


Figure 3-5. Basic IOT Instruction Format

TABLE 3-2. TYPE KV CONTROLLER INSTRUCTION SET

Octal Code	Mnemonic	Operation	Function
6051	SNC	Skip the next program instruction if the cursor interrupt flag has not been set.	This instruction senses the condition of the cursor interrupt flag. The flag produces an interrupt request when set by operation of the interrupt pushbutton on the joystick. The flag is initially cleared when the computer is started. As with all flag-sense instructions, SNC can be used under interrupt conditions to detect the source of the interrupt, or it can be used under interrupt on (ION) when the interrupt request has been caused by the operation of the cursor interrupt button. In a program running with the interrupt off, SNC can be used to ignore the cursor successive approximation subroutine in the program if a request for service has not been made from the joystick controller.
6052	CCF	Unconditionally clear the cursor flag.	This instruction is used to clear the cursor flag after a request for service has been acknowledged by the program.
6062	SAC	Select the analog comparator.	The analog comparator is set to compare the analog content of any one of six analog sources with the content of the digital-to-analog converter. The six analog sources are chosen according to a 3-bit binary code. This code establishes the parameter for choosing the wanted register according to the content of bits AC_2 AC_3 and AC_6 in the computer accumulator (refer to paragraph 3.6.4) as follows:

Accumulator Bits			*Selected Source*
2	3	6	
0	0	0	X INT
0	0	1	Y INT
1	0	0	X SH
1	0	1	Y SH
1	1	0	X CUR
1	1	1	Y CUR

TABLE 3-2. TYPE KV CONTROLLER INSTRUCTION SET (cont)

Octal Code	Mnemonic	Operation	Function
6063	LDF	Load Format.	This instruction is used to establish the mode in which a wanted graphic is to be produced according to a two-bit binary code. This code determines whether the wanted vector will be linear absolute relative, whether the point plot mode will be used or whether the cursor will be displayed. This code establishes the parameters for these formats according to the content of bits AC_2 and AC_3 in the computer accumulator (refer to paragraph 3.6.4). The LDF instruction must precede the LDX and/or LDY instructions.
6064	LDX	Load the X-axis sample and hold register.	The X-axis sample and hold register is loaded with the binary equivalent of the X-axis coordinate according to the content of bits AC_2 through AC_{11} in the computer accumulator. This data appears at the output of the digital-to-analog converter as the analog equivalent of the X-axis value of the binary word stored in the accumulator (refer to paragraph 3.6.4). The LDX instruction clears an existing ready flag and sets the ready flag after 100 ± 20 microseconds.
6065	LDY	Load the Y-axis sample and hold register.	The Y-axis sample and hold register is loaded with the binary equivalent of the Y-axis coordinates according to the content of bits AC_2 through AC_{11} in the computer accumulator. This data appears at the output of the digital-to-analog converter as the analog equivalent of the binary word in the accumulator (refer to paragraph 3.6.4). The LDY instruction clears an existing ready flag and sets the ready flag after 100 ± 20 microseconds.
6066	EXC	Execute the instruction according to the parameter word currently held in the accumulator.	Used to execute the wanted vector according to the content of bits AC_2 AC_3 AC_4 and AC_6 through AC_{11} of the computer accumulator. The parameter word establishes long or short formats circular vectors, display erasure, reset of the integrators, and intensification of the vector (refer to paragraph 3.6.4). The EXC instruction clears an existing ready flag and sets the ready flag as follows:

TABLE 3-2. TYPE KV CONTROLLER INSTRUCTIONS SET (cont)

Octal Code	Mnemonic	Operation	Function
			a. After 20 ± 5 microseconds for a point or vector continue. b. After 250 microseconds for short vectors. c. After 4.05 milliseconds for long vectors. d. After 500 milliseconds for an erase.
6071	SRF	Skip if the ready flag is set.	Used to determine when the controller is ready to perform the next execute instruction. The ready flag produces an interrupt condition when set. The flag can be set by pressing the erase pushbutton the VT01. Normally, however, the state of this flag is determined by the controller. This flag is initially cleared when the computer is started and prior to an LDX, LDY, or EXC instruction.
6072	CRF	Unconditionally clear the ready flag.	This instruction is used to clear the ready flag after a skip instruction has been acknowledged.
6073	SDA	Skip when the output of the digital-to-analog converter output is greater than the selected source.	This instruction is used in the successive approximation subroutine to determine the digital equivalent of the selected analog holding register. This instruction is used with the SAC (6062_8) instruction.
6074	LDA	Load the digital-to-analog converter.	This instruction is used to load the content of bits AC_2 through AC_{11} of the computer accumulator. This instruction is used with SDA (6073_8) in the successive-approximation subroutine to determine the digital value of the content of the selected analog holding register. This instruction does not change flag states.

equivalents of the addresses and instructions stored at those addresses. (A typical program is given in Program Example 1 at the end of this chapter.) When defining the addressable coordinates of the visible and effective image areas of the display unit, a simple decimal system can be used once the linear decimal points have been determined for the graphic construction desired. The octal value of the coordinate must be given when programming in the machine language. There are 1023/12 or 85.3 coordinates per linear inch in either the X- or Y-axis planes of the visible and effective image areas of the display oscilloscope. Hence, the desired graphic construction can be laid out on standard 10 x 10 graph paper (Dietzgen Type 340-10 or equiva-

lent, for example), each point plotted, and then these points converted to octal using the tables in the appendix. When EDGRIN is used as the source language, this conversion is performed by the assembler.

In Figure 3-6 four graphic constructions are laid out on 10 x 10 graph paper so that there is one figure in each of the four quadrants. These four figures require 13 coordinate points for their definition so that the linear equivalent of each of these 13 points must first be determined. If the linear unit distance is set to be 85 per linear inch instead of 85.3 per linear inch, a negligible error is introduced. Hence, it is only necessary to measure the distances in inches and multiply by 85 to obtain the linear coordinates of each of these points. These values are listed in the X and Y subcolumns of the Absolute Decimal column of Table 3-3. If desired, these points can be converted to relative decimal and then to octal, Absolute and Relative. There are many ways to determine the wanted coordinates; the foregoing description offers only one of many possible ways.

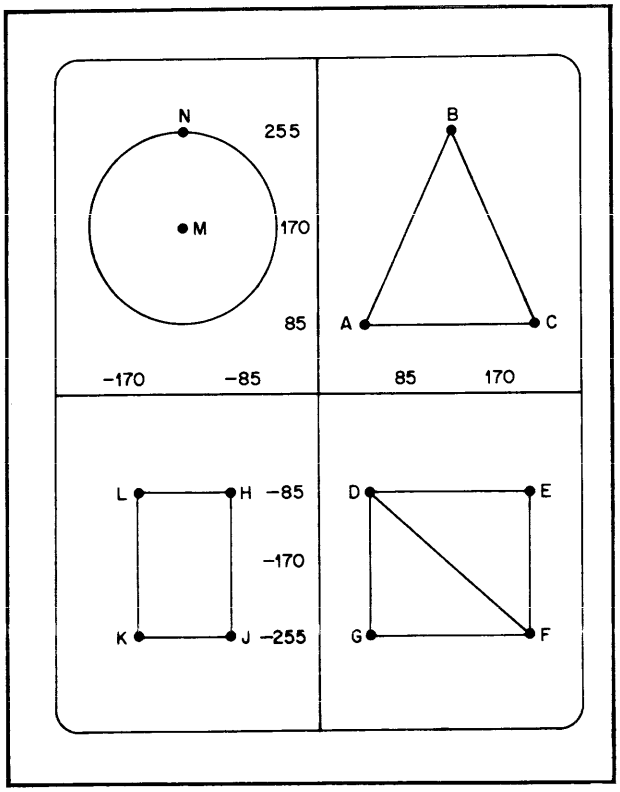


Figure 3-6. Typical Coordinate Reference System for Machine Language Programming

3.6.4 Using the IOT Instructions

The 11 IOT instructions listed in Table 3-2 comprise the complete set of machine-language instructions for the graphic display system. In some cases, the instruction operates on a word stored in the accumulator of the interfacing computer. This word may specify either a coordinate or a set of parameters for the wanted display. Any word stored in the accumulator that specifies a coordinate is considered a data word and any word that specifies parameters for the wanted display is a parameter word. The IOT instructions LDX and LDY (6064 and 6065, respectively) will accept the content of accumulator bits AC_2 through AC_{11} as data. Accumulator bit AC_2 (Figure 3-7) is the data-word sign bit. If this bit is set, the data is considered negative. Accumulator bits AC_0 and AC_1 have no meaning in the data word; the IOT instructions SAC, LDF and EXC (6062, 6063 and 6066, respectively) will accept the content of the accumulator as a parameter word. The IOT instruction LDF (6063) reads the data held in accumulator bits AC_2 and AC_3 only. The IOT instruction SAC (6062) reads the data held in accumulator bits AC_2, AC_3 and AC_6, while the IOT instruction EXC (6066) reads the data in AC_2, AC_3 and AC_4 together with bits AC_6 through AC_{11} as a parameter word (Figure 3-8).

There are two interrupt producing flags which can be sampled by separate skip tests, and one non-interrupt producing skip flag in the KV controller. A cursor interrupt flag is obtained from a pushbutton behind the joystick on the H306 joystick controller. (Refer to Table 3-1.) When the pushbutton is depressed, and if the interrupt facilities of the interfacing computer are enabled, the program currently being operated upon by the computer is interrupted. This interrupt can be used to permit the successive-approximation subroutine to be entered and a digital equivalent of the cursor or analog register to be produced in the accumulator. The successive-approximation subroutine is called for as a JMS ADCONV with the proper octal code for the source selected held in the accumulator. (Refer to ADCONV Program Example 2.) The wanted analog source is selected using the SAC instruction (listed in Table 3-2) according to the following octal code:

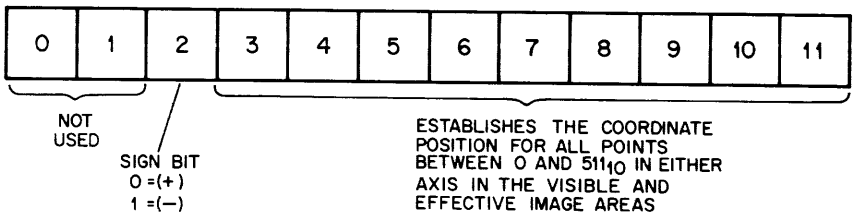


Figure 3-7. Basic Data-Word Format

TABLE 3-3. TABLE OF ABSOLUTE AND RELATIVE COORDINATES FOR FIGURE 3-6

Point	Absolute Decimal		Absolute Octal	
	X	Y	X	Y
A	43	85	0053	0125
B	128	255	0200	0377
C	213	85	0325	0125
D	43	-85	0053	1653
E	213	-85	0325	1653
F	213	-255	0325	1453
G	43	-255	0053	1453
H	-85	-85	1653	1653
J	-85	-255	1653	1401
K	-170	-255	1526	1453
L	-170	-85	1526	1653
M	-128	170	1600	0252
N	-128	255	1600	0377

Note: To specify a negative decimal number in octal, drop the sign and add 1000 to the two's complement octal magnitude. To get an octal equivalent of the two's complement, take the octal complement and add 1 to the least significant digit.

a. 0000 will select the X-axis integrator analog source.

b. 0040 will select the Y-axis integrator analog source.

c. 1000 will select the X-axis sample and hold register.

d. 1040 will select the Y-axis sample and hold register.

e. 1400 will select the X-axis coordinate of the cursor.

f. 1440 will select the Y-axis coordinate of the cursor.

The subroutine will be exited with the full two's complement answer left in the accumulator. The subroutine requires 25 consecutive locations in memory and requires approximately 900 microseconds to complete the worst case (all ones) conversion.

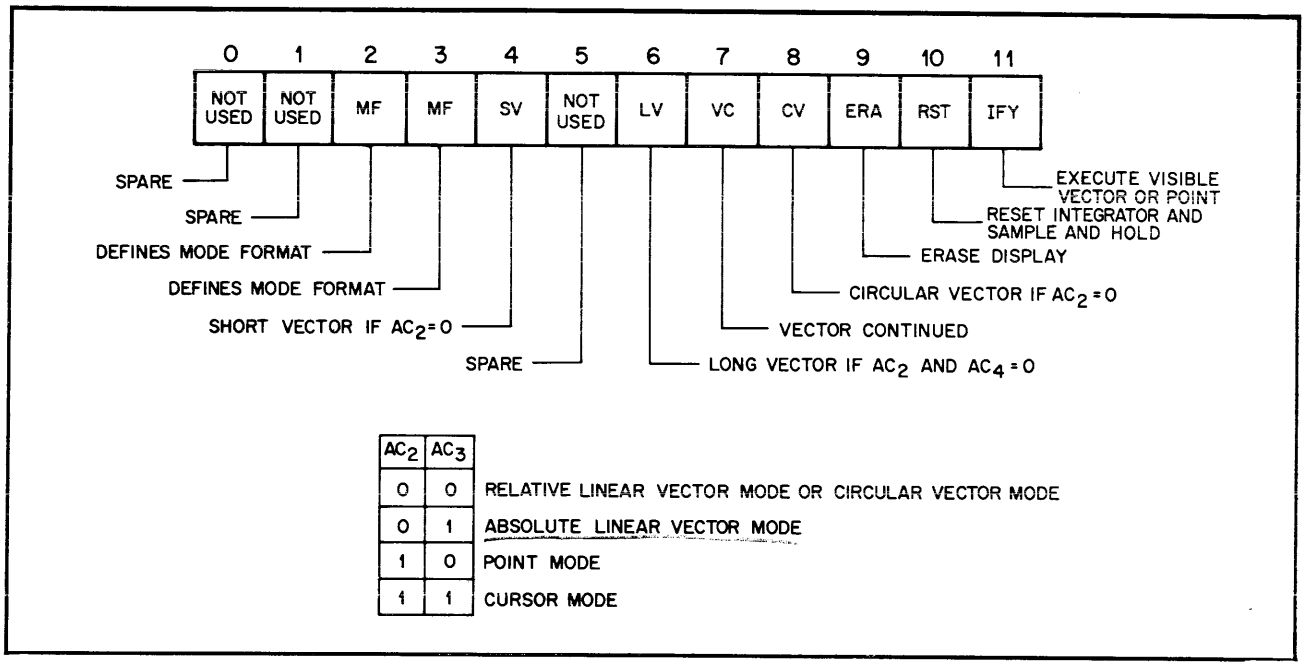


Figure 3-8. Basic Parameter-Word Formats

Program Example 1

```
JMS       DSPLY       /CALL DISPLAY SUBROUTINE WITH
          (    )      /FORMAT
          (    )      /X DATA
          (    )      /Y DATA
           - - -      /RETURN ADDRESS


DSPLY,    0
          CLA CLL             /ENTER W AC = 0 AND FORMAT, X, Y PRESET TO
          TAD I DSPLY         /DESIRED VALUES, FOLLOWING JMS CALL
          ISZ DSPLY
          6063                /LOAD FORMAT
          DCA FORMAT          /AND SAVE FOR EXECUTION
          TAD I DSPLY
          6064                /LOAD X
          CLA
          ISZ DSPLY
          6071                /WAIT FOR X TO BE LOADED
          JMP.-1
          TAD I DSPLY
          6065                /LOAD Y
          CLA
          ISZ DSPLY
          6071
          JMP.-1              /WAIT FOR Y TO BE LOADED
          TAD FORMAT
          6066                /EXECUTE THE FORMAT
          CLA
          ISZ DSPLY
          6071                /WAIT FOR COMPLETION OF EXECUTION
```

Program Example 1 (cont)

```
                JMP.-1
                JMP I DSPLY         /EXIT SUBROUTINE
FORMAT,         0                   /SAVE FORMAT
```

Program Example 2

```
/KV ANALOG TO DIGITAL CONVERSION SUBROUTINE
/CALL AS JMS ADCONV WITH SOURCE SELECTION CODE IN AC:
/0000 FOR X INTEGRATOR
/0040 FOR Y INTEGRATOR
/1000 FOR X SAMPLE AND HOLD REGISTER
/1040 FOR Y SAMPLE AND HOLD REGISTER
/1400 FOR X CURSOR
/1440 FOR Y CURSOR
/EXITS WITH FULL 2'S COMPLEMENT ANS IN AC

/REQUIRES 25 CONSECUTIVE IN PAGE REGISTERS (DECIMAL)
/APPROXIMATE 900 US TO COMPLETE THE CONVERSION WORST CASE

/SET LOCATE TO THE DESIRED ORIGIN ADDRESS

 LOCATE=200

 *LOCATE

 ADCONV,    0
            6062                /SELECT ANALOG COMPARATOR
            CLA CLL CML RTR     /+2000 IN AC
            DCA TEST            /INITIALIZE TRIAL BIT REGISTER
            TAD K7000           /INITIALIZE PARTIAL CONVERSION REGISTER
 RC1,       DCA TEMP            /SAVE PARTIAL CONVERSION
            TAD TEST
            CLL RAR
            DCA TEST            /ADVANCE TRIAL BIT
            TAD TEMP
            SZL
            JMP I ADCONV        /EXIT WHEN TRIAL BIT OVERFLOWS LINK
            TAD TEST
            6074                /LOAD D/A WITH TRIAL VALUE
            CLA CLL CML         /SET LINK
            RAR
            SNL
            JMP .-2             /WAIT 54 US
 K7000,     NOP
            TAD TEMP
            6073                /TEST D/A
            TAD TEST            /SKIPS IF TRIAL TOO LARGE
            JMP RC1             /CONTINUE

 /VARIABLES SET BY ADCONV
 TEMP,      7000                /PARTIAL CONVERSION SAVE
 TEST,      2000                /TRIAL BIT

 $
```

CHAPTER 4
PRINCIPLES OF OPERATION

This chapter of the maintenance manual covers principles of operation of the KV controller. The chapter is divided into two sections: Fundamentals of Operational Amplifiers, and Circuit Analysis. Section I provides a brief analysis of operational amplifiers and field-effect transistors (FET) as they are relevant to the understanding of the principles of operation of the KV controller. Section II is concerned with the principles of operation of the KV controller as a functional part of the KV Graphics Display System and with the principles of operation of each of the modules or functional circuits, whichever is applicable, that comprise the controller. Detail dicussions of options are not included in this chapter. The reader should refer to the list of related documents contained in the introduction to this manual for the publications covering equipments in this category.

SECTION I
FUNDAMENTALS OF OPERATIONAL AMPLIFIERS

4.1 OPERATIONAL AMPLIFIERS

An operational amplifier is basically a dc amplifier with a negative feedback loop which produces a circuit with a precise gain characteristic that depends only on the feedback used. Operational amplifiers are used in the KV controller to perform mathematical analog computations (such as addition and integration) and to provide impedance buffering for the analog outputs of the controller.

The basic requirements of an operational amplifier are: (1) the open loop gain (A), without feedback, must be very high, A = 10^4 to 10^6; (2) the input impedance must be very large to prevent loading the input signal source; (3) the output impedance must be very low for driving purposes; (4) the amplifier response time must be very short to provide a phase-gain characteristic that will allow for a strong negative feedback; (5) the bandwidth must be wide (dc to tens of kilo Hertz); and (6) offset must be low.

We will also see in the subsequent paragraphs why these characteristics are essential to the operation of operational amplifiers.

4.1.1 Idealized Operational Amplifier

The circuit shown in A, Figure 4-1 is the basic configuration of an operational amplifier. E_S and E_O represent the source and output signals,

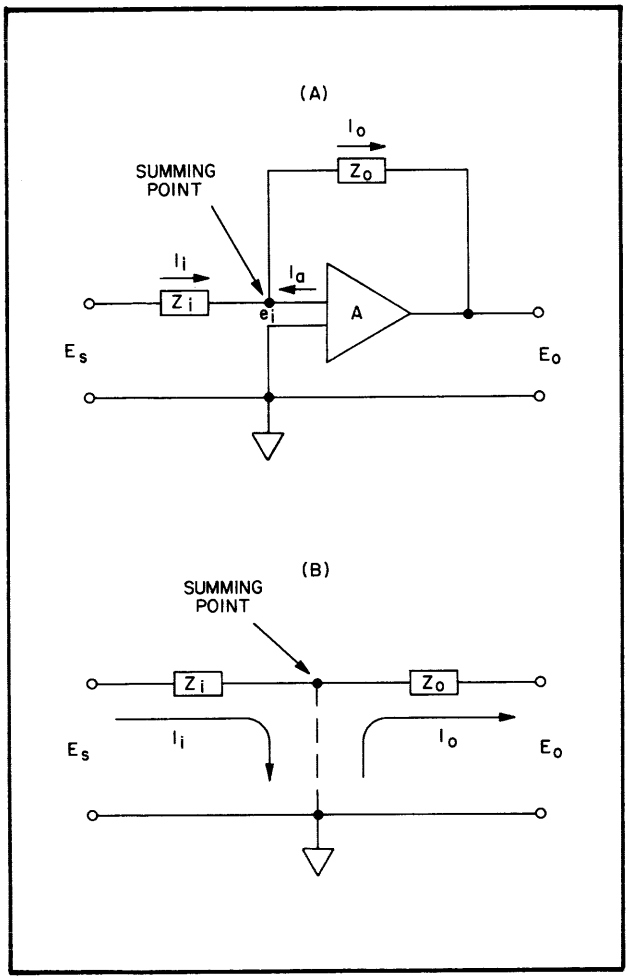


Figure 4-1. Basic Operational Amplifier, Idealized

respectively, and E_i is the resultant signal at the input of amplifier.

Assume that the characteristics of the operational amplifier are idealized and that the open loop gain (A) of the amplifier is infinite. E_i is very small compared to E_s and for purposes of this discussion we can say that no current flows into the amplifier, amplifier current (I_a) = 0. We see from the simplified diagram (B, Figure 4-1) that if $I_a = 0$, then the input current I_i and the feedback current I_o are equal placing the summing point virtually at ground potential (0 volts). In view of this we can show that the gain characteristic is dependent upon only the selected values of input and output impedances, Z_i and Z_o.

With the summing point at ground potential, equal currents flow in Z_i and Z_o.

Therefore:

$$\frac{E_s - E_i}{Z_i} + \frac{E_o - E_i}{Z_o} = 0$$

but by definition

$$E_o = A\,E_i$$

therefore,

$$E_i = \frac{-E_o}{A}$$

As A approaches infinity, E_i approaches zero and equation (1) becomes:

$$\frac{E_s}{Z_i} + \frac{E_o}{Z_o} = 0$$

or

$$\frac{E_o}{E_s} = \frac{Z_o}{Z_i}$$

However the gain of operational amplifier is defined as:

$$A = \frac{E_o}{E_s}$$

by substitution then

$$A = \frac{Z_o}{Z_i}$$

Hence, the gain characteristic of the operational amplifier is determined by the values of Z_O and Z_i components selected. From the above it is evident that when $Z_O = Z_i$ the gain of operational amplifier is unity. Unity gain operational amplifiers are used in the KV controller for impedance buffering.

4.1.2 Integrators

Operational amplifiers configured as integrators provide an output signal (E_O) that is proportional to the integral of the source signal (E_S). They are constructed by placing a capacitive element (C_O) in the feedback network (Z_O) and a resistive element (R_i) in the input network (Z_i) as shown in Figure 4-2. The time constant of the integrator is determined by the selected values of the resistor and capacitor. The current through the feedback loop (I_O) charges the capacitor and the stored charge (E_O) is seen by the load on the integrator as the integral of the source signal (E_S), which is:

$$E_O = \frac{1}{R_i C_O} \int E_s dt$$

If the input voltage is a constant (dc), E_O is a ramp equal to

$$E_O = \frac{E_s t}{R_i C_O}$$

the amplitude of the ramp (E_O), as we can see, is directly dependent upon the time (t) the capacitor is permitted to charge.

4.1.3 Scaling Adder

The scaling adder is used in the digital-to-analog converter and the sample and hold analog registers of the KV controller. As shown in Figure 4-3, the adder, basically, comprises a precision resistive ladder network with *n* number of pre-

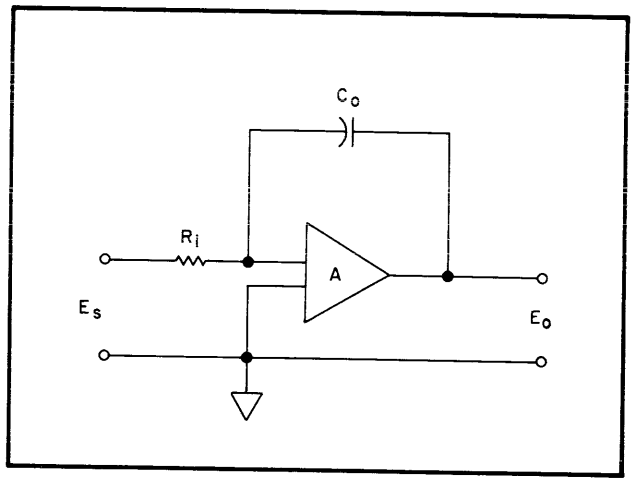


Figure 4-2. Integrator, Basic Configuration

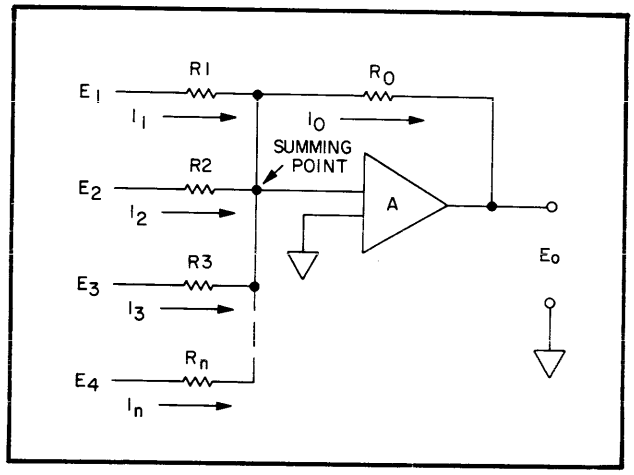


Figure 4-3. Scaling Adder, Basic Configuration

cision resistors as the input impedance (Z_i) and a precision resistor for the feedback impedance (Z_O). In this type of adder each input is seen at the summing point as the input resistance (Z_i). Assuming that the summing point is idealized (virtually at ground potential or 0 volts) each input is multiplied by a constant (which is determined by the value of the resistor in each leg of the resistor ladder) before summing-inverting; and the input current (I_i) at the summing point is, therefore, equal to the algebraic sum of the current in each leg of the precision resistor ladder network. Hence, if I_i equals I_O then

$$I_O = \frac{E_O}{R_O} = I_1 + I_2 + I_3 \cdots\cdots + I_n$$

and the output voltage (E_O) equals

$$E_o = -R_o\left(\frac{E_1}{R_1} + \frac{E_2}{R_2} + \frac{E_3}{R_3} + \cdots \frac{E_n}{R_n}\right)$$

Input signals E_1, E_2, etc. in the application of the scaling adder in the D/A converter are applied from a common reference source (E_S) and E_O is only dependent upon the resistances selected. The above formula in this case becomes

$$E_o = -R_o E_s\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \cdots \frac{1}{R_n}\right)$$

However, in its SH application, input voltages (E_1 and E_2) are applied from two distinct sources, D/A output and reference supply, and E_O in this case is dependent upon both input voltage and resistance (R_1 and R_2).

$$E_o = -R_o\left(\frac{E_1}{R_1} + \frac{E_2}{R_2}\right)$$

4.2 FIELD-EFFECT TRANSISTORS

4.2.1 General

The field-effect transistor (FET) is a unipolar transistor which has broad applications as a sampling gate for multiplexer switching and other switching functions. Ideally, switches should introduce zero impedance into a circuit when closed and should exhibit infinite impedance when open. Relay switches approximate this ideal situation; however, when high-speed switching is required, electromechanical devices are too slow and must give way to the use of solid state switches, such as FET's.

Convention bipolar transistor switches in the "on" state exhibit a small impedance, and in addition an offset voltage which, in the case of the controller switches, is in series with the signal source. In some applications this offset voltage is negligible; however, when dealing with low-level analog signals in the millivolt range it can be troublesome. FET's have the important advantage of having effectively no offset voltage. The FET, when in the "on" state, appears to the signal source as a simple ohmic resistor; not a resistance in series with an offset voltage. As it is used in the controller, the FET introduces no error due to offset making it ideally suited for its application here.

4.2.2 Application

Consider now the circuit shown in Figure 4-4. (It should be noted that the circuit shown is typical of the FET switches and drivers used in the controller.) The FET (Q16) is a series sampling gate, in series with the signal source (V_S) and the load (R_L). Driver Q1 controls the state of FET and is normally off due to the biasing arrangement established by resistors R_1 thru R_3.

The resultant -15V at the collector of the driver maintains the FET in "off" or open state and the FET appears to the signal source as a very large resistor, in the order of megohms; hence, the path to the load is open. Upon command of the timing circuits, a negative-going signal is applied to the driver and the driver conducts causing a 15-volt transition at its collector. The FET alters state; and in the *on* or *closed* state, the FET appears as a small resistor (175 to 350 ohms) establishing a low impedance path for the signal source (V_S) to the load. The potentiometer in series with FET permits adjustment of the resistance exhibited at the input of the operational amplifier when the FET is on. The period that the FET is on is determined by the time duration of the gating pulse which, in turn, is established by the timing circuits of the KV controller.

The 15-volt amplitude of the gating pulse exceeds the required gating specifications to ensure that the FET remains in the on state for the duration of the gate.

The limitations of the FET, as it is used here, are VS must not exceed the breakdown voltage of the FET, and the speed of the FET, when compared with other solid state switching devices, is relatively slow (2 microseconds switching time, typical). The former limitation is a very important precaution to be observed in troubleshooting the KV Controller. Quite often

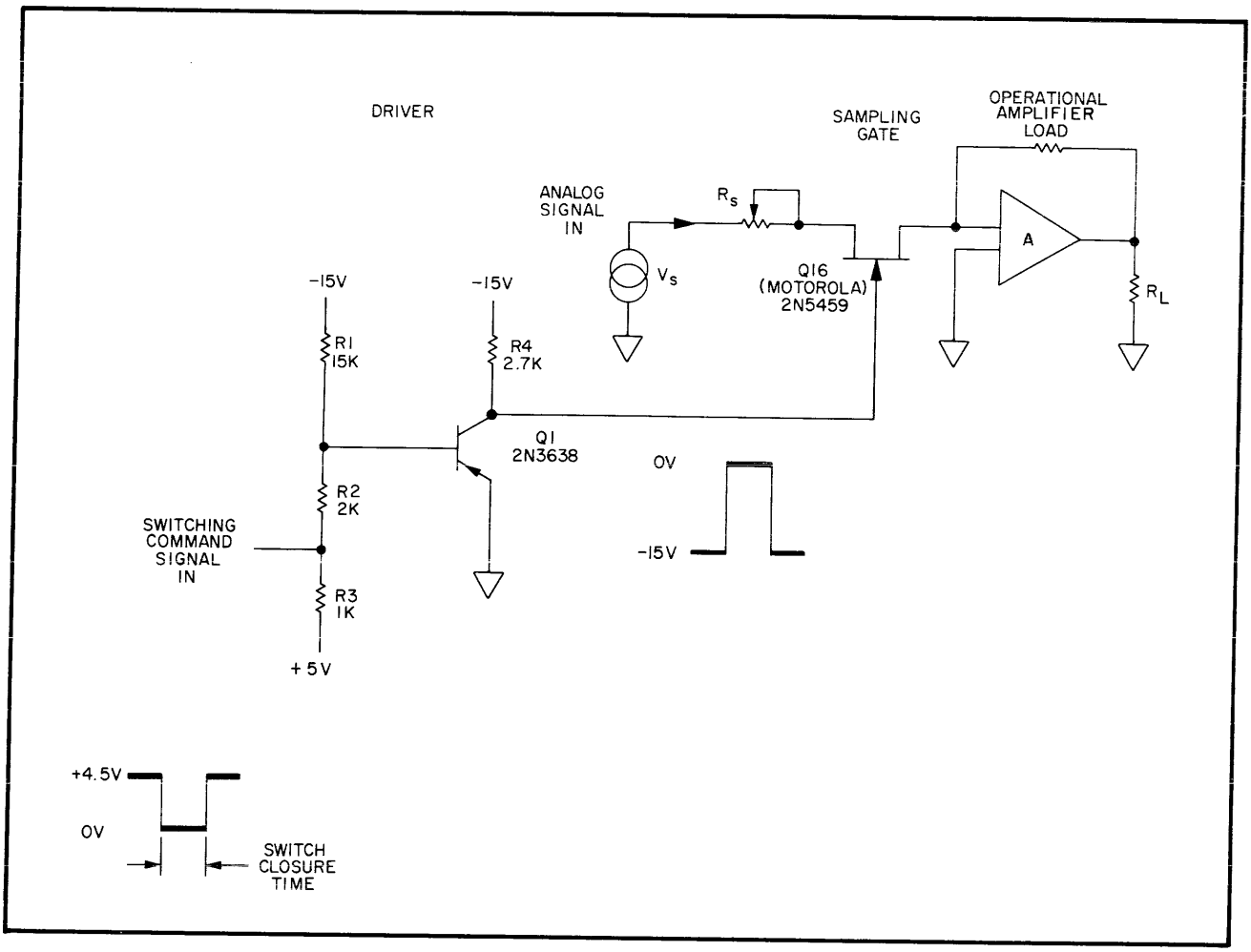


Figure 4-4. Typical KV Controller, FET Switching Circuit with Driver

failures of FET's are caused by excessive inverse voltage across their terminals.

4.3 SAMPLE AND HOLD

A SH register can best be described as an analog storage device; i.e., it stores an analog signal indefinitely, assuming there is no drift or leakage. For simplicity, we can consider a sample and hold as a capacitor to ground (in the controller the capacitor is connected to the summing point or virtual ground of an operational amplifier) that is impedance isolated by an input buffer amplifier with a switch (FET), which disconnects it from the capacitor after the capacitor has charged.

Figure 4-5 illustrates a simplified version of the SH. Amplifier Q1 is the input buffer amplifier and has unity gain (the input and feedback resistors have the same value). Hold switch S1 (FET), when closed, permits application of the analog data to be stored. The length of time S1 is closed is determined by the time duration of the gating signal; hence the timing circuits. During the period S1 is closed, capacitor C charges to the value of the analog input signal. The charge on the capacitor is held on the one side by the high impedance of the open hold switch and on the other by the low output impedance of holding amplifier Q2.

When a new value is to be stored, S1 is closed. If the value of the analog signal is lower than the previously stored value, the capacitor will discharge to the new value of the analog signal. If the value of the analog signal is greater, then the reverse occurs.

In the KV controller, a FET is connected across the capacitor for reset purposes. The FET is

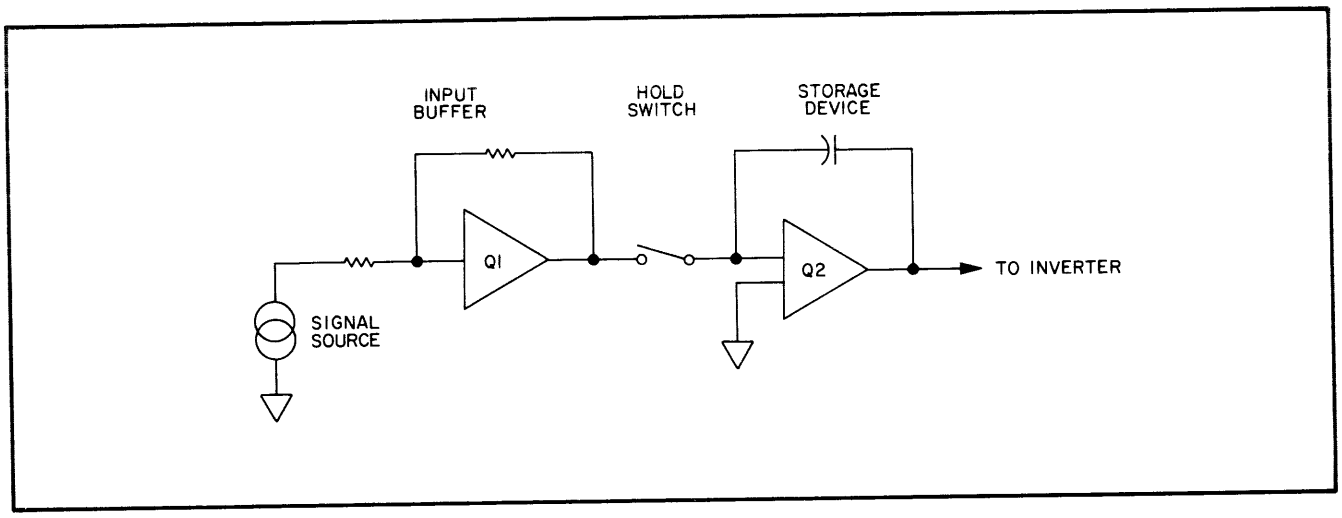


Figure 4-5. Sample and Hold Analog Register, Simplified Schematic Diagram

normally open and leakage through it is negligible since it exhibits such an extremely high impedance in this state. However, when it is closed, a low impedance discharge path (approximately 175 ohms) to ground is provided and the capacitor; hence the SH, is reset.

SECTION II
SYSTEM ANALYSIS

4.4 GENERAL

The KV Controller is divided into three major functional groups as indicated in Figure 4-6: IOT control and timing, digital-to-analog converter and gate control logic and the analog function generator. The I/O control and timer is responsible for all communications with the computer. It accepts inputs from the accumulator (via the appropriate IOT instruction) and communicates back to the computer via the skip and interrupt bus only. The D/A converter and gate control accepts inputs from one or more of the internal hardware registers and generates the appropriate analog and digital control signals to the analog function generator (AFG). The AFG comprises the major control portion of the system and produces the actual X and Y deflection voltages necessary to display lines, arcs, points or the cursor from the H306 Joystick Controller onto the surface of the VT01 Storage Tube Display Unit.

In addition to the analog output capabilities of the AFG, the system includes an analog comparator which can be selected to perform, via the appropriate software program, a 10-bit analog-to-digital (A/D) conversion upon one of four possible internal analog sources and one of two external analog sources, normally representing the output position of the joystick controller. The resolution of the D/A is one part in 1024 ± 1/2 least significant bit. The overall accuracy of the A/D process is one part in 256.

4.4.1 Internal Digital Registers

There are four internal input registers, two interrupt producing flag registers, and four internal timing registers. The D register is a 10-bit data register used to hold the data during a load data instruction and also to hold part of the microprogrammed execute instruction. The PT, AB, and L/S registers are one-bit control registers used to establish and maintain the necessary *permanent* paths within the AFG to perform the desired function. These three registers are also used to select the source and initialize the comparator for use in performing A/D conversions.

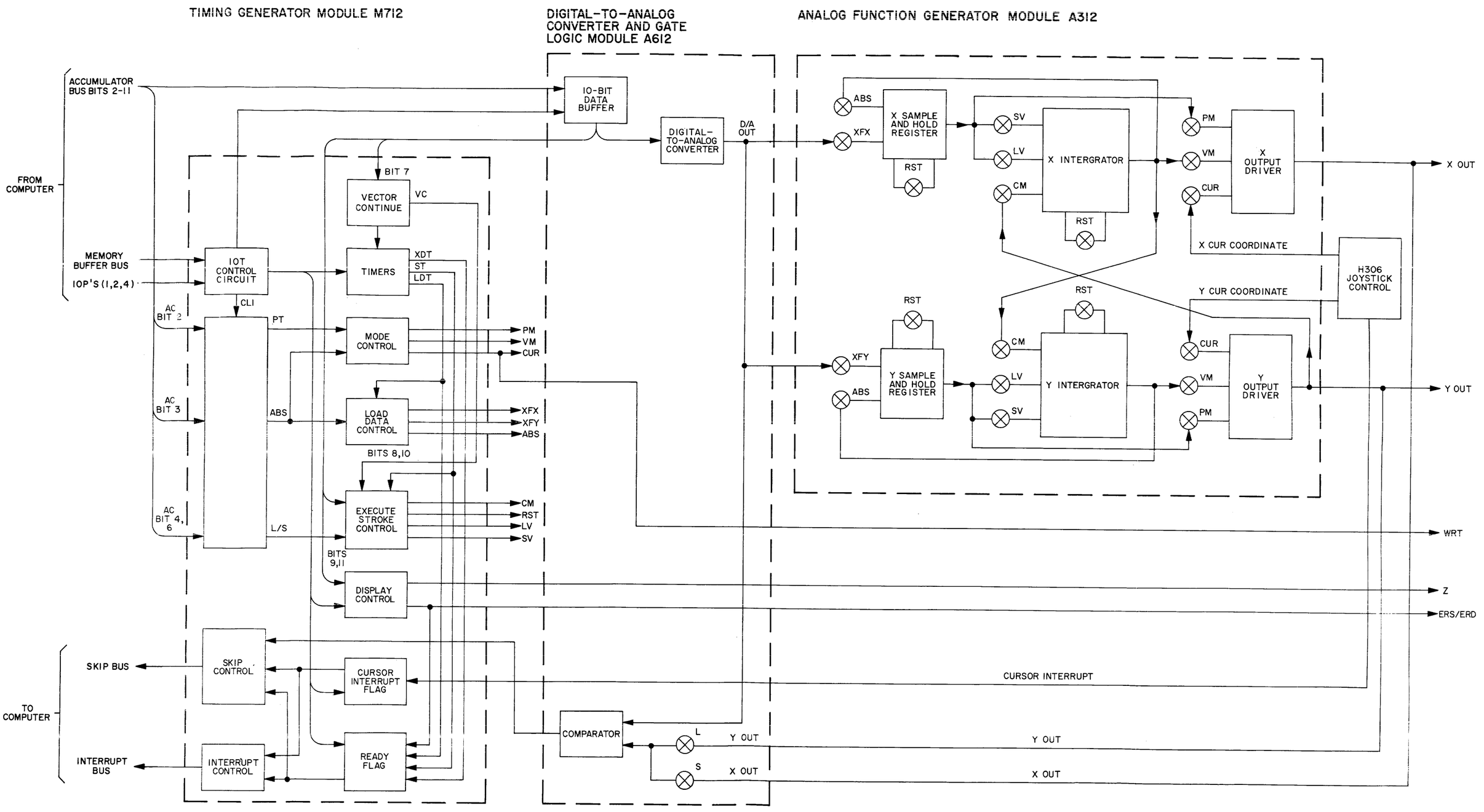


Figure 4-6. KV Controller Functional Block Diagram

The KV control contains two flags which are gated to the interrupt bus. The cursor interrupt flag is raised upon pressing the interrupt button on the H306 Joystick controller. The ready flag is raised either by pressing the erase button on the VT01, or upon completion of any load or execute operation. Both flags are initially cleared when the computer is started.

There are four internal timing sources in the KV control and these determine the duration of a given operation as denoted by the setting of the ready flip-flop. The load data timer (LDT) is set nominally to 100μs ±20μs and represents the time necessary to load data. The execute delay timer (XDT) is set to 20μs ±5μs and is activated by an execute command. This timer will set the ready flip-flop at the completion of a point plot command or at the start of a vector continue (VC) command only. For all other execution commands it initiates the stroke timer (ST). This latter unit will time out precisely to 2700 machine cycles (1.5μs each or nominally 4 milliseconds) or exactly 1/16 this time (250 microseconds), depending on the setting of the long/short vector (LS) register. The ST will set the ready flip-flop at the completion of its operation. The last internal timing register, the VC, is activated by the XDT at its completion and inhibits the ST, replacing the precise hardware timing function with a timing function which can be scaled under direct program control. The VC is only activated when enabled by AC bit 7 at execute time.

4.4.2 Digital-to-Analog and Analog-to-Digital Conversion Facilities

The D/A converter in the KV controller transforms the contents of the D register into a nominal 0 to -4 volt analog signal with an overall resolution of one part in 1024. The analog comparator accepts a ±1-volt analog signal, multiplies it by 2 and adds -2 volts to make it become 0 to -4 volts, and then compares this against the analog output of the D/A converter, producing a high output if the D/A is more negative in voltage than the suitably scaled unknown, and producing a low output if the opposite is true. This comparator output is sampled by a skip instruction and the resultant skip/no skip condition is used to create a digital image of the unknown analog signal in the AC by a successive-approximation program.

4.4.3 Analog Function Generator

The AFG basically operates like a hybrid computer, combining the properties of an analog computer with digitally selected signal paths. There are 10 input digital control signals, which establish the signal paths and the mode of operation of the KV controller, and four analog input signals applied to the AFG. There are two analog output signals which are produced as a result of the input signals. These signals are listed in Tables 4-1 and 4-2.

4.5 CONTROL CIRCUITS

4.5.1 Input/Output Transfer Control

The Input/Output Transfer (IOT) control circuits shown in Figure 4-7 interface directly with the I/O bus of the computer and accept Memory Buffer (MB) levels and Input/Output Pulses (IOP) to logically form the necessary IOT instructions which are subsequently used to prime gates for the generation of the internal

TABLE 4-1. ANALOG FUNCTION GENERATOR, INPUT/OUTPUT SIGNALS

Analog Input Signals	Range	Source
XDA	0 to -4V	D Register
YDA	0 to -4V	D Register
XCUR	± 1V	X Position of joystick
YCUR	± 1V	Y Position of joystick

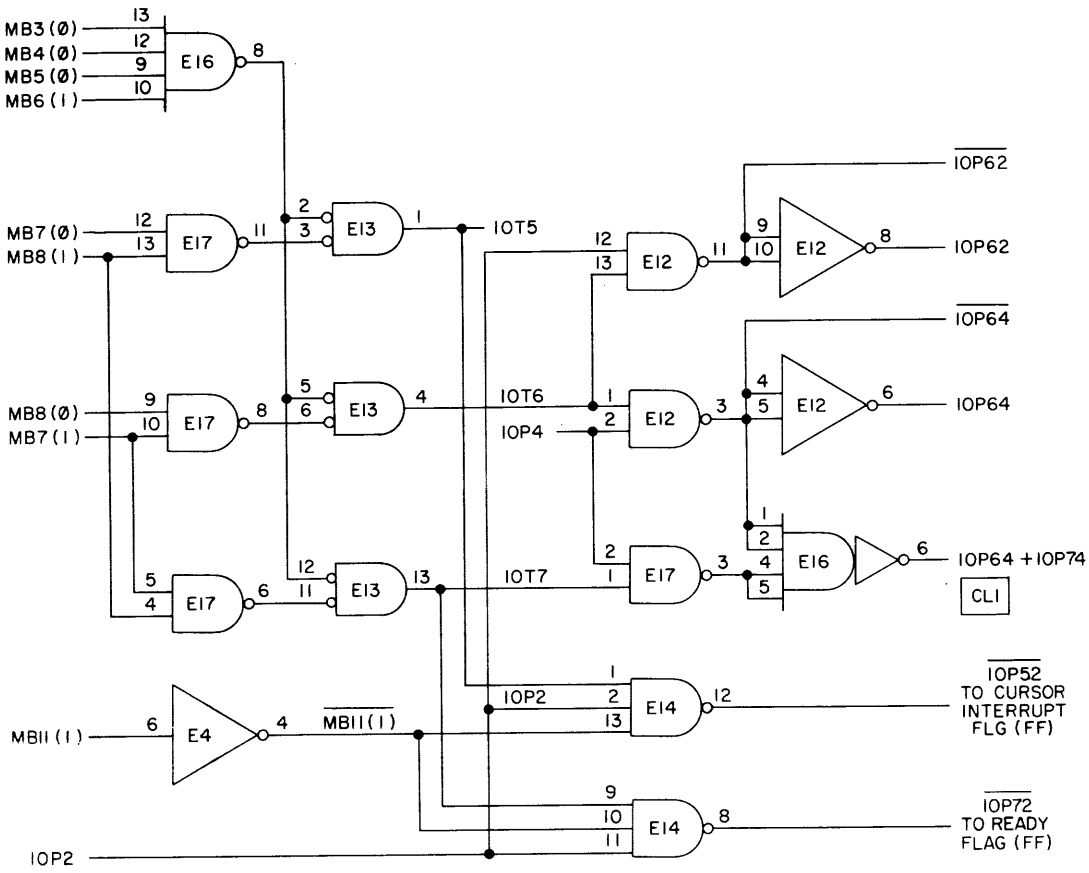


Figure 4-7. IOT Control Circuit, Logic Diagram

TABLE 4-2. ANALOG FUNCTION GENERATOR, DIGITAL CONTROL SIGNALS

Signal	Action or Use
OUTPUT PATH	
PM (Point Mode)	Closed in point plot mode to connect the SH registers to the VT01
VM (Vector Mode)	Closed in vector mode to connect the INTH registers to the VT01
CUR (Cursor Mode)	Closed in cursor mode to connect and display X CUR and Y CUR from the H306 joystick off-line as a non-stored elliptical pointer.

TABLE 4-2. ANALOG FUNCTION GENERATOR, DIGITAL CONTROL SIGNALS (cont)

Signal	Action or Use
	INPUT PATH
ABS (Absolute Mode)	Closed only during a load data operation to load data from the D register as *absolute* data.
XFX (Transfer X)	Closed to load the X sample and hold register from XDA. Data is interpreted according to the state of ABS during load time.
XFY (Transfer Y)	Closed to load the Y sample and hold register from YDA. Data is interpreted according to the state of ABS during load time.

IOP execution commands and to perform other control functions. The IOT instructions, IOT5, 6, and 7, are logically formed by NAND gates E17A-C and E16A and NAND gates E13A-C from levels MB3 through 8. The IOT levels are used to prime NAND gates for generation of execution commands at the event time of the IOP's from the computer. (See Figure 4-8.) The internal IOP execution commands are IOP52, 62, 64, 72, and 74 and perform the following control functions:

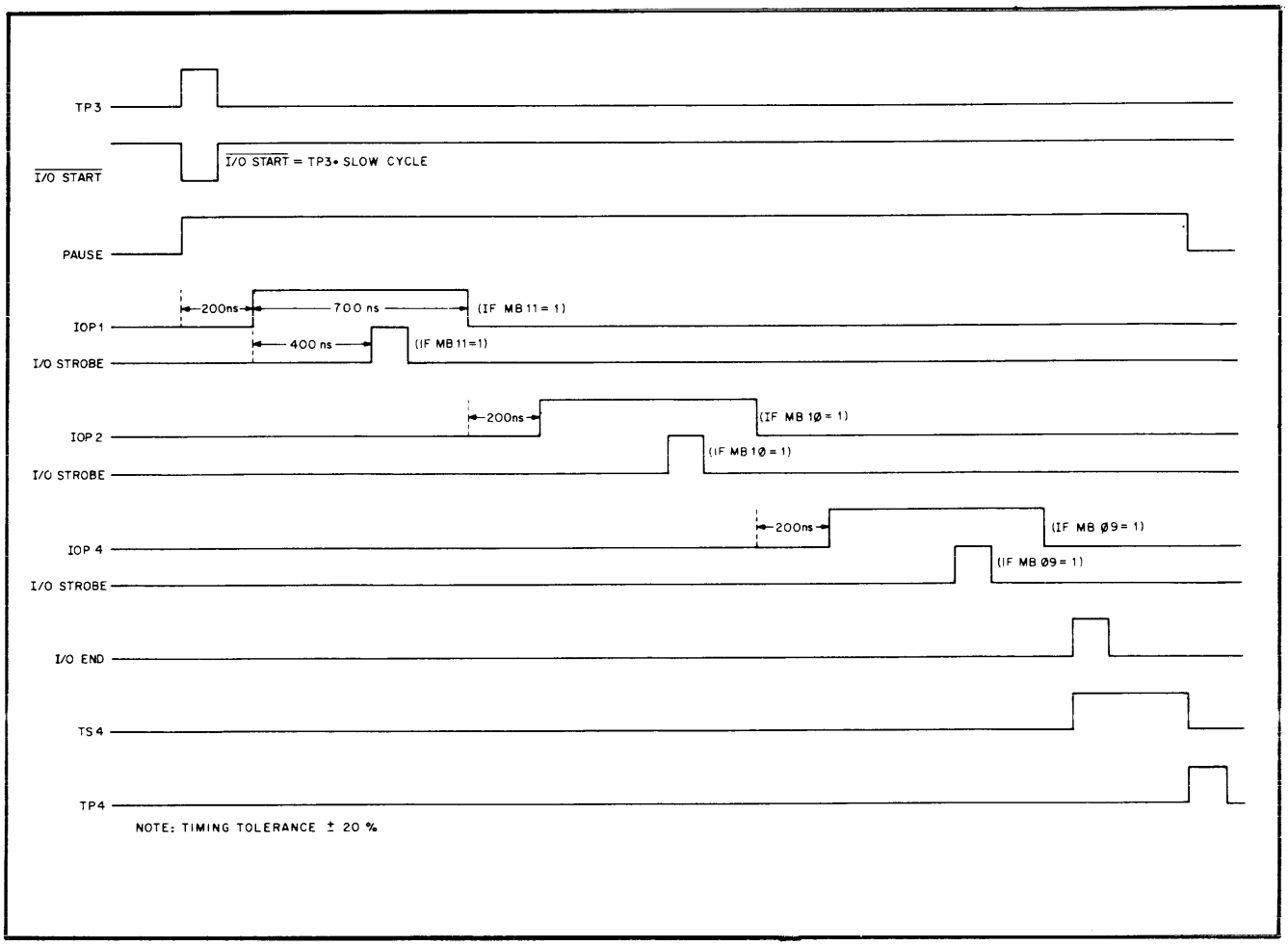


Figure 4-8. IOP Timing Diagram

IOP52 Resets the Cursor flip-flop.

IOP62 Resets the ÷16 Counter and PASS and Vector Continue flip-flops in vector mode. Clocks PT and AB registers which establish the permanent path (mode of operation) of the AFG. Clocks LONG/SHORT vector flip-flop.

IOP64 Resets the READY flip-flop. Sets the PASS flip-flop from the conditions established on the L/S flip-flop. Initiates the LOAD DATA Timer (D1) if MB 10 = 0, or the EXECUTE DELAY TIMER (d2) if MB 10 = 1. Forms the clock pulse to load the D register from the accumulator.

IOP72 Resets the Ready flip-flop.

IOP74 ORed with IOP64 to form the CLOCK pulse to load the D register.

4.5.2 Skip and Interrupt Control Facilities

The KV controller communicates with the computer via the skip and interrupt circuits of the timing generator. The circuit consists of CFL and READY flip-flops E19A and E19B, six logic gates (E18, E20A, E20B, E21A, E21B, and E22) and Interrupt bus driver Q2 and Skip bus driver Q1. When either CFL or READY flip-flop is set NAND gate E18 is enabled and an interrupt command is applied to the computer. A skip command is executed when any one of the four NAND gates of the skip circuit is primed and an IOP1 command is applied. IOP72 and IOP52 execution commands reset the READY and CFL flip-flops, respectively.

4.6 TIMING CIRCUITS

4.6.1 Load Data Timer

The LDT circuit shown in Figure 4-9 establishes the time, 100 ±20 microseconds, to load the output of the D/A into the X and Y SH registers of the AFG. The LDT is primed by MB10 (1) and initiated by execute command IOP64 which also clocks B1 flip-flop E10. Depending upon the setting of B1 flip-flop E10, the LDT (1) output is applied to either the XFY Driver Q1 or XFX Driver Q2 to load the Y or X SH register, respectively. When the B1 flip-flop E10 is set, MB11 (1) is high, NAND gate E5C is primed and the Y SH register is loaded. When the B1 flip-flop is reset (MB11 (1) is low) NAND gate E5D is primed and the X SH register is loaded. At the completion of each LDT function, the LDT (0) output is applied to skip and interrupt control circuit to set the READY flip-flop. The LDT is also used to load data in the absolute mode when NAND gate E2 is primed by AB (1). (AB is set by IOP62 generated during a 6062, 6063, 6066 or 6067 instruction.)

4.6.2 Execute Delay Timer

The XDT E9, shown in Figure 4-10, provides a delay of 20 ±5 microseconds and is actuated by execute command IOP64. The XDT (1) output sets the READY flip-flop in point mode by enabling NAND gate E7C which is already primed by level PT + B7 in this mode. When the KV controller is in a VM level, PT + B7 is low and the XDT (1) output is used to initiate vector timing functions.

4.6.3 Long and Short Vector Timing Circuit

The vector timing circuit shown in Figure 4-10 provides two hardware timing functions: long vector, approximately four milliseconds, and short vector, approximately 250 microseconds. Both timing functions are initiated by XDT E9 which starts the ST consisting of series connected monostables E2 and E1. The ST introduces a 250-microsecond delay each time it is pulsed. In long vector mode the ST will time out after it has cycled sixteen times. In short vector mode the ST times out after one cycle.

Long Vector Timing

In this mode the L/S and PASS flip-flops are set. Bit AC4, which is used to prime NAND gate

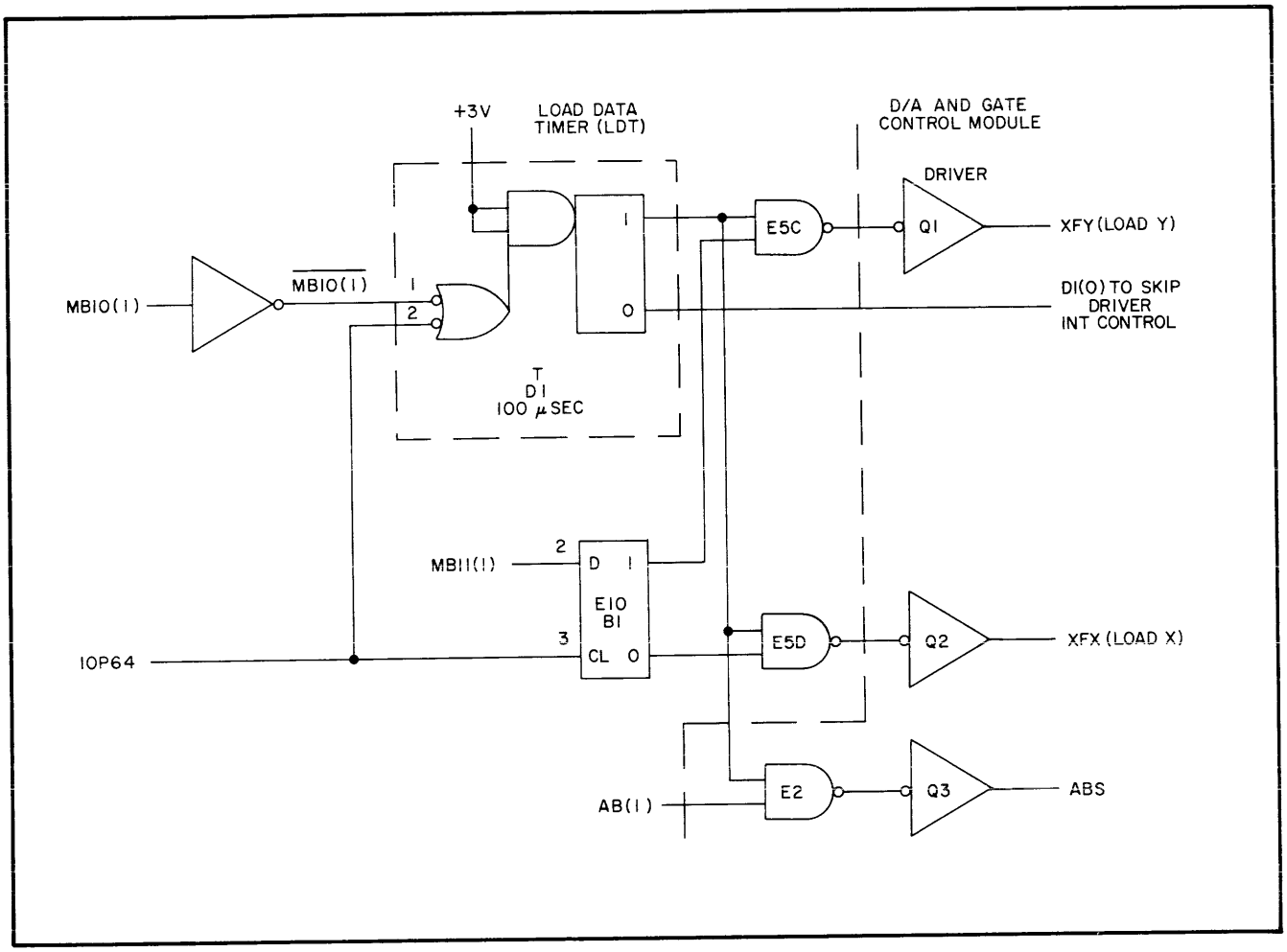


Figure 4-9. Load Data Timer (LDT), Simplified Logic Diagram

E15A directly and NAND gate E6A after inversion by inverter E15B, is low. Execute command IOP62 sets the L/S flip-flop and resets the ÷ 16 Counter. The L/S (1) output along with AC4 (1) primes NAND gate E6A and is ANDed by execute command IOP64 to set the PASS flip-flop. The Pass (1) output of the flip-flop primes NAND gate E5B which establishes the necessary preconditioning for long vector timing. The XDT (1) from the XDT is applied to pin 10 OR gate E7D to initiate the ST and to enter one count into the ÷ 16 Counter. This cycle is repeated until 16 counts are entered into the counter. After the sixteenth pulse, the counter resets the PASS flip-flop which, in turn, disables NAND gate E5B and the Pass (0) output primes NAND gate E5A. The final ST (1) output, which occurs approximately 250 microseconds after the PASS flip-flop is reset is ANDed with the Pass (0) output by NAND gate E5A to set the READY flip-flop. The output of disables NAND gate E5B and the Pass (0) output primes NAND gate E5A. The final ST (1) output, which occurs approximately 250 microseconds after the PASS flip-flop is reset is ANDed with the Pass (0) output by NAND gate E5A to set the READY flip-flop. The output of the ST in this mode is a positive going level four milliseconds in duration which is taken at the 0 output of each of its monostables and applied to OR gate E6B. The output of the OR gate is integrated by resistor R17 and capacitor C20 to filter out the spikes caused by the propagation delay time in cycling and the delay in triggering of monostable E1 by monostable E2.

Short Vector Timing

In this mode the L/S and PASS flip-flops are reset; hence, NAND gate E5B is inhibited and NAND gate E5A is primed. After the ST is

initiated as described in the previous paragraph, the ST will time out after one cycle and set the READY flip-flop since there is no return path to the ST.

4.7 DIGITAL-TO-ANALOG AND ANALOG-TO-DIGITAL CONVERSIONS

4.7.1 Digital-to-Analog Converter

The D/A converter, shown in Figure 4-11, produces an analog voltage that corresponds to an applied 10-bit binary word, accumulator bits AC2 through AC11. The data word conversion corresponds to the following:

Data Word (octal)	Analog Voltage
1000	0V
0000	-2V
0777	-4V

The circuit consists of a 10-bit buffer, a precision resistor network and operational amplifier K1. The buffer stores the data word from the accumulator. The precision resistor network, consisting of resistors R68 through R77, is a binary weighted summing network with R68 representing the most significant bit and R77 the least significant bit.

The precision resistor network and operational amplifier comprises a scaling adder such as the one described in paragraph 4.1.3 with a common source voltage. The input current (I_i) seen at the input of the operational amplifier is, therefore, the algebraic sum of the current in each leg of the precision resistor network; and from the same discussion, the input current is equal to the output or feedback current. Hence, the output current is the analog equivalent of the data word stored in the buffer. The operational amplifier establishes the signal range and converts the output current signal to a voltage signal.

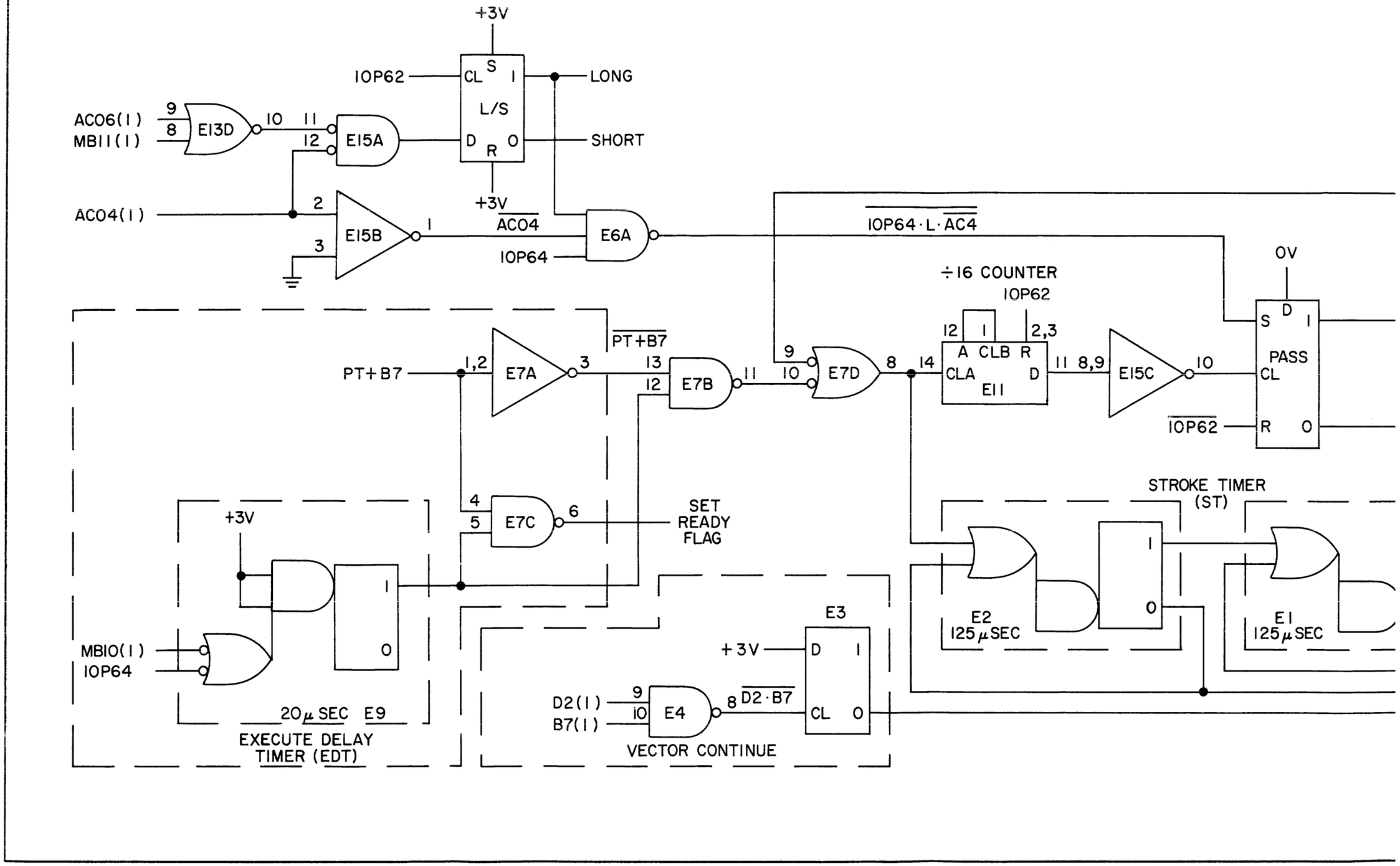
The transistors, Q13 through Q22, in each leg of the precision resistor network, equate the binary levels of each of the flip-flops of the buffer. [Transistors Q13 through Q22 are specially selected, matched transistors operating in an inverse mode as saturating switches. Replacement of a faulty transistor will require replacement of an entire set of four (Q13 - Q17 or Q18 - Q22). The specifications on these transistors are listed on the circuit schematic for the A612 in Chapter 7.

4.7.2 Analog-to-Digital Converter

By adding a comparator, a NAND gate (skip control) and a clock, as shown in Figure 4-11, the D/A converter discussed above becomes a successive approximation type A/D converter which converts the X and Y analog outputs of the AFG to a 10-bit binary word. The D/A converter operates by repeatedly dividing the possible input voltage (AFG output) in half and making a bit-by-bit comparison starting with the most significant bit to determine its digital value. This comparison is accomplished by algebraically summing the output of the D/A (0 to -4 volts) and the output of the AFG (±1 volt) at the inverting input of comparator K2 and comparing it to a ground reference at the non-inverting input. Each leg of the comparator is precisely weighted to compensate for the disparity in the voltage range of the AFG output and the output of D/A converter. (The cause of this disparity will be discussed later in the description of the sample and hold.) When the algebraic sum of the two signals is less than ground (D/A output is less than or equal to the AFG output), the comparator produces a positive output which primes skip control, NAND gate E20A. Through the successive approximation subroutine, instruction 6073, the bit is entered and stored in the AC.

4.8 SAMPLE AND HOLD

As previously discussed the SH register is an analog voltage storage device which upon a load data command charges to a dc voltage value corresponding to the output of the D/A; hence, the data word stored in the input buffer register. The output of the D/A ranges from 0 to -4 volts. The analog value stored in the SH, however,


+3V
IOP62
CL
S
1
L/S
D
R
0
LONG
SHORT
AC06(1)
MB11(1)
9
8
E13D
10
11
12
E15A
AC04(1)
2
3
E15B
1
+3V
AC04
IOP64
E6A
IOP64·L·AC4
0V
÷16 COUNTER
IOP62
12
1
2,3
A CLB R
CLA
D
E11
11 8,9
E15C
10
S
D
1
PASS
CL
R
0
IOP62
PT+B7
PT+B7
1,2
E7A
3
13
12
E7B
11
9
10
E7D
8
14
STROKE TIMER
(ST)
4
5
E7C
6
SET
READY
FLAG
+3V
1
0
MB10(1)
IOP64
20μSEC E9
EXECUTE DELAY
TIMER (EDT)
E3
+3V
D
1
CL
0
D2(1)
B7(1)
9
10
E4
8
D2·B7
VECTOR CONTINUE
E2
125μSEC
E1
125μSEC

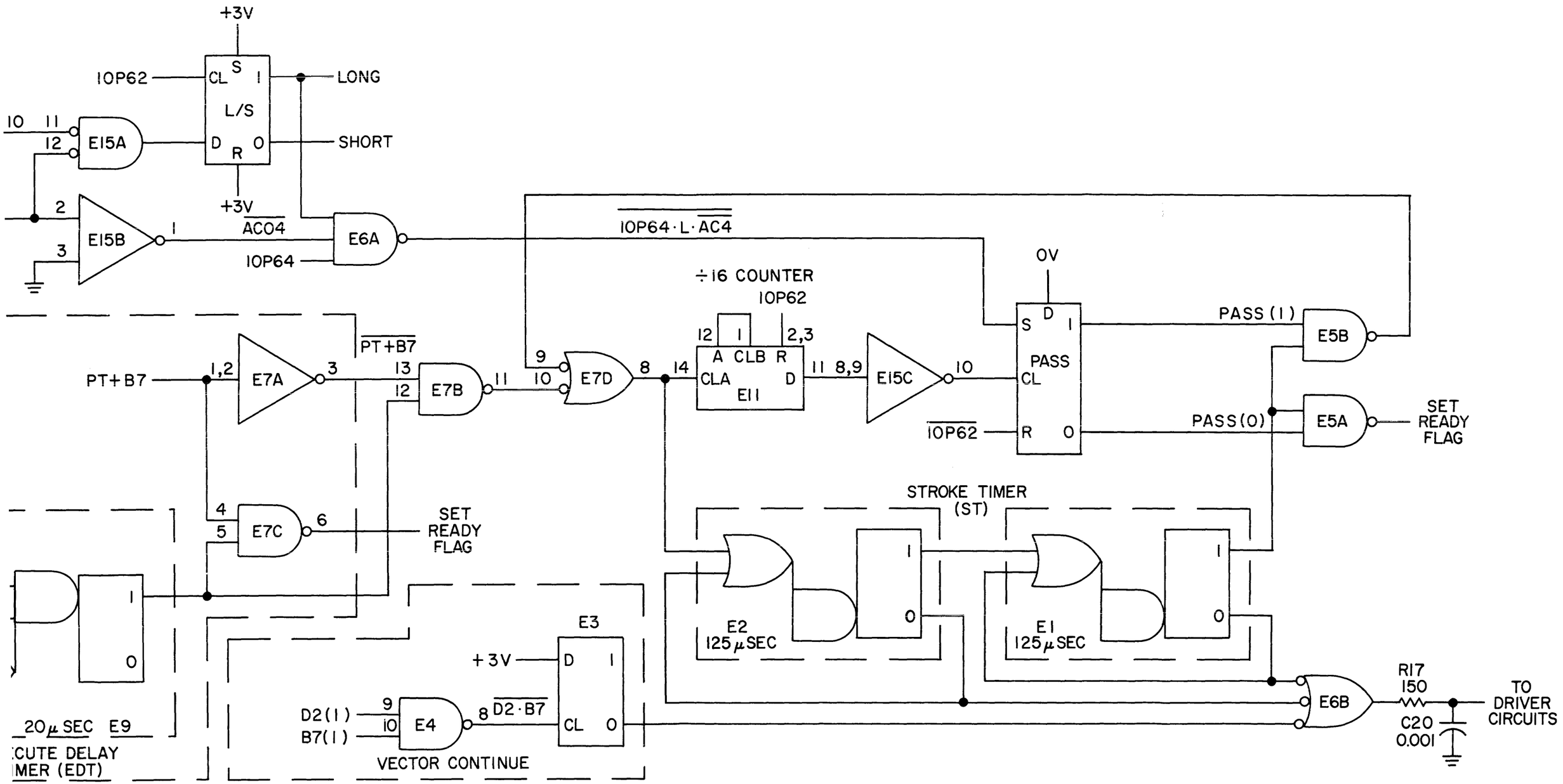


Figure 4-10. Execute Delay Timer, Long/Short Vector and Vector Continue Timing Circuit, Simplified Logic Diagram

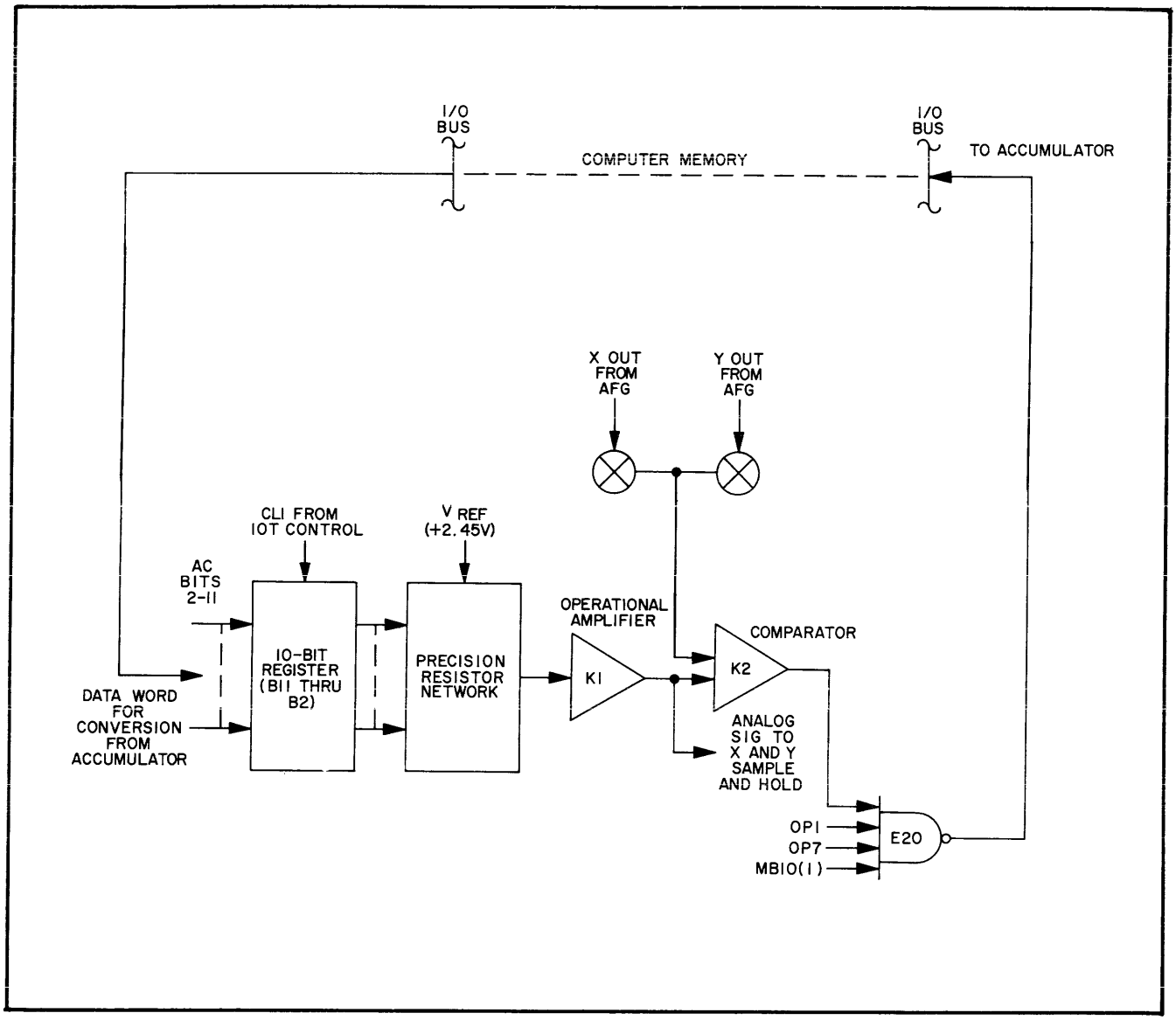


Figure 4-11. Digital-to-Analog/Analog-to-Digital Converter, Functional Block Diagram

ranges from -2 to +2 volts. The relationship of the data word stored in the input data register and the respective output of the D/A and the value stored in the SH is:

Data Word (octal)	D/A Voltage	S and H Voltage
1000	0	+2
0000	-2	0
0777	-4	-2

We shall see in the subsequent detail discussion how this transition is accomplished.

The circuit configuration for both the X and Y SH is identical; therefore, only X SH is covered in this discussion. When an X load data command is applied to Q1 (hold switch), the switch closes providing a low inpedance path for output of input buffer E1 to E2. Capacitor C1 (storage capacitor) charges to the applied voltage level. The stored charage on C1 is reflected back to the input (E1) through inverter E3 and R5.

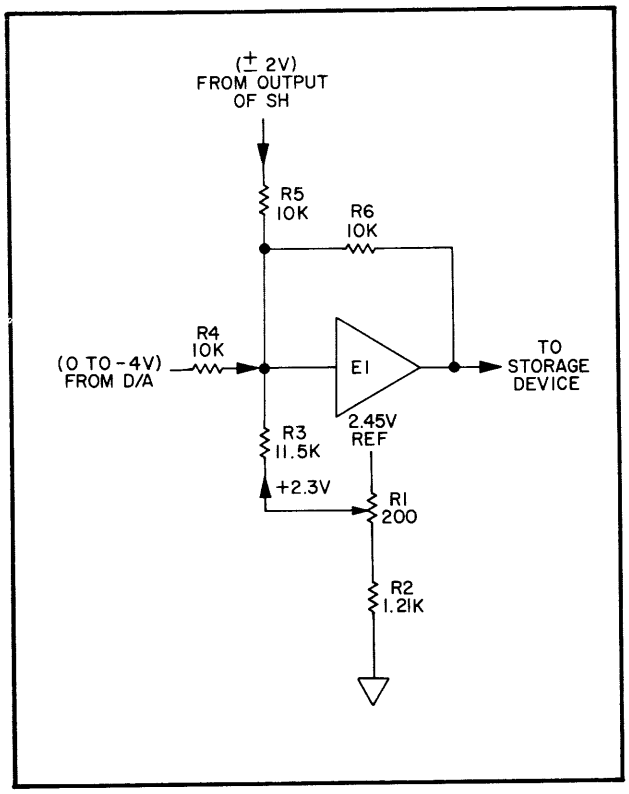


Figure 4-12. Sample and Hold Register Input Buffer, Simplified Schematic Diagram

Input buffer E1 is a three-input adder as shown in Figure 4-12. The input seen at E1 is the algebraic sum of the output of D/A (R4), SH feedback (R5) and +2.3-volt reference voltage (R3) which is established by the biasing arrangement of R1 and R2. Initially, assuming the SH has been reset, the feedback input is 0 volts. The input is, therefore, the algebraic sum of the D/A output and reference supply. If we refer to formula (4) or paragraph 4.1.3, we see that the reference voltage and the value of R3 are so selected to cause the output of E1 to range from +2 to -2 volts in direct proportion with the 0 to -4 volt output range of the D/A.

As previously discussed the charge on C1 is reflected back to the input, making R5 another leg in the summing network. (Refer to paragraph 4.1.3.) The reflected signal tends to maintain the output of E1 at 0 volts by reflecting back a current corresponding to the amount of drift in the SH, thus maintaining the voltage held by the SH at the analog equivalent of the word stored in the D/A buffer.

The above discussion assumed that the ABS FET gate (Q4) was open. Hence, the ouptut of the SH equals the D/A voltage with +2 volts added. This is the required method of loading the SH for point mode, circular vector mode, and linear relative vector mode.

For absolute linear vector mode, however, the ABS FET Q4 will be closed during the load data period. Under these conditions, the holding output of the X integrator (E4) will be inverted by E3 and subtracted from the equivalent ±2v D/A input voltage by adder E. Thus, the SH output will charge to a value equal to the equivalent D/A input voltage minus the present voltage on the integrator. See paragraph 4.11.2 for a discussion of how this voltage produces absolute linear vectors.

4.9 INTEGRATORS

The integrator circuit shown in Figure 4-13, upon an SV or LV command, integrates the analog value stored in the associated X or Y SH. E4 and E9 are the X and Y integrators, respectively. The integrators are isolated by their respective input and output FET's, therefore, the charge on the integrating capacitors, C2 (X) and C6 (Y), are effectively stored values. For the operation of integrators, refer to paragraph 4.1.2.

4.10 OUTPUT DRIVERS

The output drivers are unity-gain operational amplifiers. E5 and E10 are the X and Y output drivers, respectivley. The input impedance to each of the amplifiers consists of a resistor and a FET. The resistance exhibited by the FET, when closed, and the value of fixed resistor is approximately equal to the respective output resistor.

4.11 MODES OF OPERATION

4.11.1 Point Mode

In the point mode of operation, FET's Q9 and Q25 are closed and the analog value stored in the X SH and Y SH are applied directly to input of their respective output drivers, bypassing the integrators.

4.11.2 Vector Mode

In a vector mode of operation VM FET's Q11 and Q24, which place the output X and Y

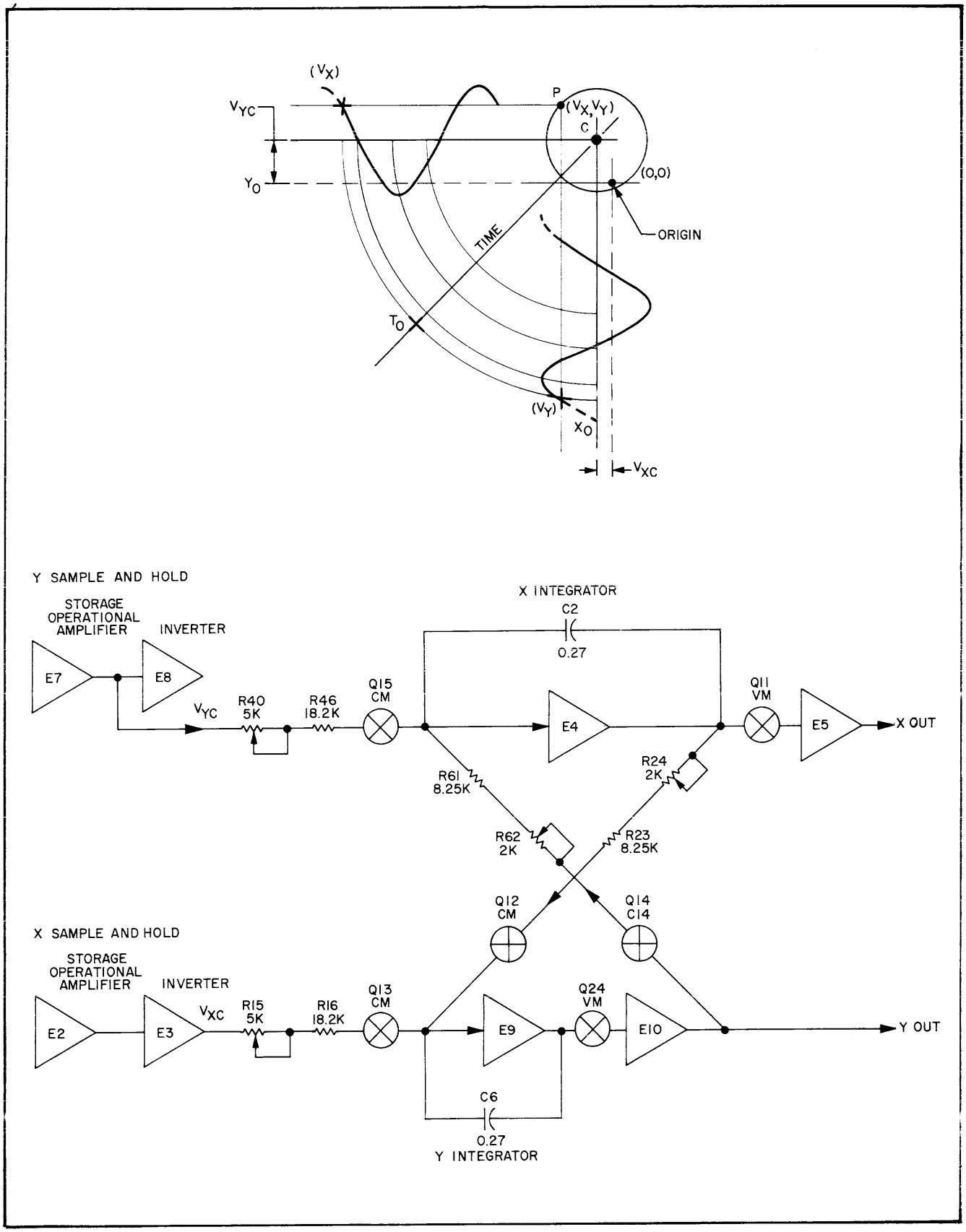


Figure 4-13. Analog Function Generator in Circle Mode Configuration and Circle Generation Geometry

drivers in circuit with either the SH registers or both, are closed. In this mode, the analog function generator generates either linear or circular vectors.

Linear Vectors

In a linear vector mode, all stages of the AFG are in circuit and the AFG may generate either long (4.08 milliseconds) or short (275 ±10 microseconds) vectors. In long vector mode, Q5(X) and Q21(Y) FET's are closed to connect the SH to the integrator. In short vector FET's Q6 and Q22 are closed for the same purpose.

In the linear vector mode, the Analog Function Generator processes either relative or absolute vectors. In relative linear vector mode the voltage on the SH, ΔX_{rel}, equals the corrected input D/A voltage, XDA. The integrator adds this voltage to its present holding value of X_0 to achieve the new holding value X_1 (the end point of the vector). This end point thus equals:

$$X_1 = X_0 + X_{rel} = X_0 + XDA$$

Thus, XDA represents a relative increment to the present position of the integrator.

In absolute linear vector mode, the voltage on the SH, ΔX_{ABS}, equals the corrected voltage from the D/A, (XDA), less the present voltage held on the integrator, i.e.,

$$X_{ABS} = XDA - X_0$$

The integrator again adds this voltage to its present holding value of X_0 to achieve the end point voltage X_1:

$$X_1 = X_0 + \Delta X_{ABS} = X_0 + XDA - X_0 = XDA$$

Thus, the new end point equals the corrected D/A input voltage directly, producing an absolute address.

Circular Vectors

A circle or arc pattern is displayed on the screen of the display unit when the X and Y inputs are sinusoidal signals 90 degrees out-of-phase with one another, i.e., the X and Y inputs are functions of the sine and cosine, respectively. If both the X and Y signals are referenced to 0 volts, the circle is described about the origin (0, 0) or center of the viewing screen. On the other hand, if either one or both signals are referenced to some offset voltage, the circle is described about the coordinates established by the offset voltage. Figure 4-13 illustrates the relationship of the coordinates of the center of the circle with respect to the origin and the X and Y input signals. Point P represents the circle starting point. V_{xc} and V_{yc} are the offset voltages that determine the center of the circle.

Obviously, the circuit required to generate a circle or arc pattern is an oscillator capable of providing two outputs at the same frequency that are 90 degrees out-of-phase with one another and capable of being offset. This is precisely the circuit configuration of the AFG in the circle mode of operation.

In the circle mode of operation, the analog function generator initially operates in a linear vector mode and stores a set of coordinates in the X and Y integrators that corresponds to a point on the circumference of the circle or arc. The coordinates of the center of circle or arc are then stored in the X and Y SH registers. The difference in the value stored in the integrators and the SH is the radius of the circle. With both sets of coordinates stored a circle mode command is applied and the circle configuration of the analog function generator in the mode of operation is as shown in Figure 4-14. The circle mode FETs (Q12 through Q15) and vector mode FETs (Q11 and Q24) are closed. As shown, the X and Y integrators are cross-coupled to form a low frequency oscillator whose frequency is dependent upon the RC network formed by the respective integrator capacitor and the resistance in the cross-coupling network, resistors R24 and R23 for the X integrator and resistors R61 and R62 for the Y integrator along with the closed resistance of the respective FET's. (The potentiometers permit adjustment of the resistance in the coupling network to compensate for the variation in resistance exhibited by the closed FETs in series.)

The coordinate of the center stored in the Y SH register (taken at the output of the storage operational amplifier and bypassing the inverter E3) biases (offsets) the summing point of the X integrator through scaling resistance R15 and R16; X output from the SH register (taken at output of the inverter E8) biases the Y integrator through the scaling resistance of R40 and R46. Consider now the instant the center mode FET's are closed (Figure 4-13), the output of the X integrator ($\int I_X$) appears at the summing point of the Y integrator. The output of the Y integrator is, therefore, the sum of the second integral of I_X and the first integral of I_Y. The Y integrator output is inverted by Y output driver E10 and appears at the summing point of the X integrator closing the oscillator loop. The statement above can be made starting at the output of the Y integrator and tracing through the X integrator, so that both X and Y coordinates are double integrated and provide the necessary coordinates of a circle.

4.11.3 Cursor Mode

In cursor mode, FET's Q10 and Q26 are closed and the output (position) of the joystick (±1V) is applied directly to the respective X and Y driver. (See Figure 7-3.) In this mode of operation the coordinates of the position of the joystick can be converted to 10-bit binary words and stored in the AC by the A/D process described in paragraph 4.7.2 and, subsequently, placed in the respective SH for line drawing, if desired.

4.12 POWER SUPPLIES

The KV controller contains two regulated power supplies (nominally +11.5 and -11.5 volts) both of which are contained in the A712 Voltage Regulator Module. (See Figure 7-4.) Primary ac power (center tapped 28 volts ac) is supplied to the module from an external step-down transformer. The module contains a full-wave bridge rectifer, two type LM300 regulators (one for each supply) and two series pass transistors. Transistors Q1 and Q3 are the respective +11.5 and -11.5 volt series pass transistors. A booster transistor, Q2 is included in the negative supply to drive series pass transistor Q3. The output regulation references of the respective supplies are set by resistors R2 and R3 and resistors R4 and R5. Transistor Q4 and resistors R6 through R9 provide current limiting for the negative supply. Capacitors C8 through C10 filter the unregulated dc output of the bridge rectifier. Capacitors C3, C6, C11, and C12 provide filtering of the regulated output voltages.

CHAPTER 5
MAINTENANCE

This chapter is divided into two sections: Introduction and System Maintenance. Section I covers information concerning the Digital Equipment Corporation's warranty and service policies and maintenance concepts. Section II covers alignment and adjustment, trouble analysis, preventive and corrective maintenance.

SECTION I
INTRODUCTION

5.1 WARRANTY

5.1.1 Modules and Accessories

Type B, R, W, M, K and A Modules

All B, R, W, M, K and A Modules shown in Catalog C-105, as revised from time to time, are warranted against defects in workmanship and material under normal use and service for a period of ten years from date of shipment (providing parts are available). DEC will repair or replace any B, R, W, M, K, or A modules found to be defective in workmanship or material within ten years of shipment for a handling charge of $5.00 or 10% of list price per unit, whichever is higher. Handling charges will be applicable from one year after delivery. Notwithstanding anything herein contained to the contrary, the Module Warranty outside the continental U.S.A. and Canada is limited to repair or replacement of the module and excludes all costs of shipping, customs clearance, or any other related charges.

System Modules

All System Modules, Laboratory Modules, High Current Pulse Equipment, G, S, H, Non-Catalog Flip-Chip Modules and Accessories are warranted against defects in workmanship and material under normal use and service for a period of one year from date of shipment. DEC will repair or replace any of the above items found to be defective in workmanship or material within one year of shipment. Handling charges are available to the purchaser upon request. Notwithstanding anything herein contained to the contrary the Module Warranty outside the continental U.S.A. and Canada is limited to repair or replacement of the module and excludes all costs of shipping, customs clearance, or any other related charges.

5.1.2 Shipping

All modules must be returned prepaid to the Digital Equipment Corporation. Transportation charges covering the return of the repaired modules shall be paid by the Digital Equipment Corporation except as required by paragraph 5.1.1. The Digital Equipment Corporation will select the carrier, but by doing so will not thereby assume any liability in connection with the shipment nor shall the carrier be in any way construed to be the agent of the Digital Equipment Corporation. Please ship all units to:

Digital Equipment Corporation
Module Marketing Services
Repair Division
146 Main Street
Maynard, Massachusetts 01754

No module will be accepted for credit or exchange without the prior written approval of DEC, plus proper Return Authorization number.

5.1.3 Systems

Systems are warranted against defects in workmanship and material under normal use and service, as discussed below, for a period of three (3) months from the date of installation. Notwithstanding the aforesaid, in the event that DEC is prevented by causes beyond its control from properly installing the equipment, the period for this warranty shall be deemed to commence on the thirtieth (30th) day after delivery, or upon installation, whichever is sooner. DEC's sole responsibility under this warranty shall be, at its option, to either repair or replace any component which fails during this period; providing the purchaser has promptly reported same to DEC in writing and DEC has, upon inspection, found such components to be defective. The purchaser must obtain shipping instructions for the return of any item under this warranty provision. Compliance of such instructions shall be a condition of this warranty.

5.1.4 Other Warranty Conditions

All above warranties are contingent upon proper use in the application for which the products were intended and do not cover products which have been modified without DEC's approval, or which have been subjected to unusual physical or electrical stress or on which the original identification marks have been removed or altered. These warranties will not apply; (i) if adjustment, repair or parts replacement is required because of accident, neglect, misuse, failure of electric power, air conditioning, humidity control, transportation or causes other than ordinary use, or (ii) if the equipment is installed by the customer without prior written approval from DEC, or (iii) if the equipment is removed from its location of initial delivery.

5.2 SERVICE POLICY

Unless explicitly agreed upon by the owner and the Digital Equipment Corporation, the responsibility for preventive and corrective maintenance, after warranties have elapsed, lies solely with the owner of the Type KV Storage Tube Control Unit. Replacement stockpiles, special tools, test equipment, or other auxiliary equipment listed as a requirement for maintenance in this manual, will not be supplied by the Digital Equipment Corporation.

5.3 MAINTENANCE CONCEPT

Maintenance is divided into two categories: preventive and corrective. Preventive maintenance is performed periodically to ensure that the equipment is operating properly. Corrective maintenance, on the other hand, is performed whenever a failure occurs in the course of normal operation. In either case, the KV Controller is connected in a system configuration and is subjected to a rigorous diagnostic self-test routine for detection of improper or marginal operation, in the case of preventive maintenance, and for the localization and subsequent isolation of equipment failures, in the case of corrective maintenance.

It should also be noted that the information presented in this chapter assumes that maintenance personnel understand the operation of the central processor unit (CPU) and other peripherals and options on line with the system;

and, in addition, are familiar with the programming and operation of the CPU as described in the applicable Computer User Handbook and in Chapter 3 of this publication.

SECTION II
SYSTEM MAINTENANCE

5.4 PREVENTIVE MAINTENANCE

5.4.1 General

The preventive maintenance procedures for the KV Controller consists of visual mechanical inspection and running the diagnostic test routine to check for marginal operation and system calibration. Mechanical inspection consists of checking module seating, clearing, and visual inspections. The diagnostic checks are intended to isolate any marginal circuit condition or intermittent failures so that they can be corrected.

Operators or maintenance personnel should record data obtained during preventive maintenance in a log book. Analysis of this data can indicate the rate of circuit deterioration and component degradation so that steps can be taken to prevent system failure.

The periodicity of mechanical inspection should be at least once a month, particularly cleaning to allow efficient functioning of cabinet air filters. The diagnostic routine should be performed every 600 equipment operating hours or every three months whichever comes first. Appreciable changes in the temperature-humidity environment of the system may require the performance of the diagnostic self-test routine and recalibration of the system.

5.4.2 Mechanical Inspection

Perform the following mechanical inspection of the system to ensure efficient operation:

a. Clean the exterior and the interior of the equipment using a vacuum cleaner.

b. Visually inspect the equipment for completeness and general condition. Repaint any scratched or corroded areas.

c. Inspect all wiring and cables for cuts, breaks, fraying, wear, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace, as required, any defective wiring or cable covering.

d. Inspect the following components for security: switches, connectors, and capacitors. Tighten or replace as required.

e. Inspect all module mounting panels to ensure that each module is securely in its connector.

f. Inspect module components for overheating, breaks and faulty solder connections. Repair as required.

5.4.3 Diagnostic Testing and Minimum Performance Tests

Minimum performance tests for the KV Controller are based on the diagnostic program and the procedures given below. When the minimum performance requirements of the graphic display system are checked the program exercises the system and detects a KV Controller malfunction and a visual examination of each display indicates apparent abnormal operation of the controller or display. The KV Controller diagnostic routine is based on the assumption that there is no malfunction in either the interfacing computer or in the display unit. If the minimum performance check is not successful, a calibration check should be made.

Whenever a malfunction of the KV Controller is detected, the diagnostic routine will halt. If the

program halts, the address register on the interfacing computer console should be consulted. The address at which the program halts provides a key to the apparent malfunction. Accompanying the diagnostic routine is a listing of the halt addresses and a description of the corresponding fault.

Method

Using the binary loader, load diagnostic self-test tape MAINDEC-8I-D6 CE-D-(D) into memory and select starting address 200_8 using the switch registers on the computer console and then start the program. If a program halt occurs, consult the Action column of the diagnostic routine. For any halt between address 0173_8 and 0442_8 refer to the troubleshooting procedure in paragraph 5-5.

NOTE

Because there are no IOT control circuit calibration procedures, a halt at any address between 0173_8 and 0442_8 is caused by an apparent malfunction in the computer or in the KV controller control circuit.

5.5 TROUBLE ANALYSIS

Trouble analysis consists of, essentially, isolating failures to a module of the KV Controller with the diagnostic routine. Although the diagnostic routine provides a complete overall check of the system, there may occur troubles where the actual module that is causing the failure cannot readily be isolated. The subsequent paragraphs are intended to supplement the diagnostic routine in locating the cause of such failures.

5.5.1 Power Supply

A power supply failure is manifested by a complete failure of the analog circuits. To check the input to, and the output from, the power supply, connect a voltmeter to the following pins and monitor the voltage at each pin:

Pin	*Voltage*
AC Input	
H21R2 to H21N2	28 ± 2.8 V
DC Output	
J25E1 to Ground	+11.5 ±1 V
J25B1 to Ground	-11.5 ±1 V

NOTE

There exist two distinct grounds in the KV controller, analog and digital ground. Care must be taken in the selection of the proper ground when performing measurements on the KV controller.

If the a-c input to the power supply is not within tolerance, the transformer is at fault. If the d-c output of the power supply is not within tolerance, the power supply is at fault.

5.5.2 Analog Faults

It is virtually impossible for the diagnostic routine to determine whether the D/A Converter and Gate Control Logic Module or the Analog Function Generator Module is at fault when an analog halt instruction is encountered. To determine which module is at fault, the iterative features of the diagnostic routine and an oscilloscope or a voltmeter can be used to isolate the trouble. The Switch Register must be set to the applicable address and the analog and applicable gate control signals monitored at the interface of the two modules. (See figure 5-1.) If either the analog or gate control output signals of the D/A Converter is abnormal, the module should be replaced. If the output signals are normal, the Analog Function Generator Module should be replaced.

5.5.3 Joystick Controller

To check the joystick controller, connect an oscilloscope or a voltmeter to the output terminals indicated in Figure 5-1 and measure the

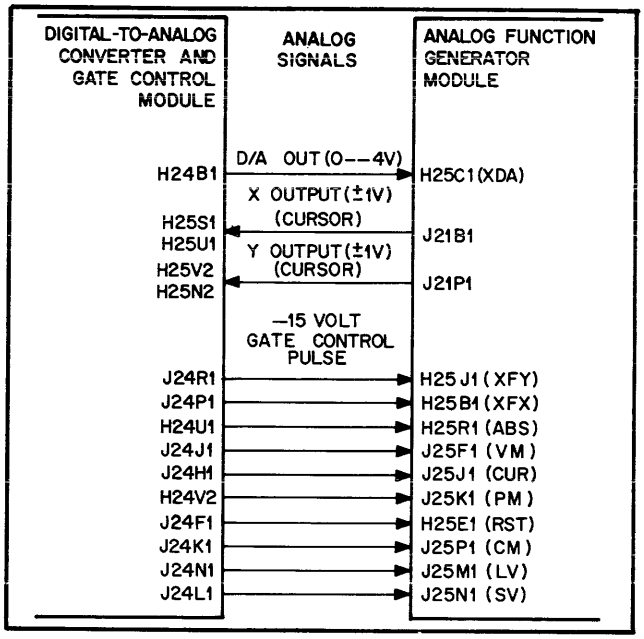


Figure 5-1. Digital-to-Analog Converter and Gate Logic Module/Analog Function Generator Module Interface

voltage in each axis while operating the joystick through a full sweep in both the X and Y axes. The voltage in both the X and Y axes should range from -0.5 to +0.5 volts for full screen deflection.

5.5.4 Component Part

Troubleshooting to a component part may be necessary when a replacement module is not readily accessible or when a customer desires to maintain his equipment. To troubleshoot to a component part, the iterative features of the diagnostic routine along with an oscilloscope or a voltmeter can be used to signal trace digital levels and pulses and analog signals to isolate a trouble to a component part. Reference should be made to the logic diagrams contained in Chapter 7 and the parts location diagrams in Chapter 6 when signal tracing. The module under test must be installed onto Module Extender W983 for access to test points. Use standard shop practices to remove and replace component parts.

5.6 ALIGNMENT AND ADJUSTMENT

There are 27 potentiometers contained in the KV Controller which require adjustment when the equipment is initially installed or after replacement of a component part of module. The display unit must be on line with the controller, and the diagnostic self-test tape (MAINDEC-8I-D6 CE-D(D)) loaded into the CPU. Maintenance personnel need only to run the diagnostic routine, as described in paragraph 5.4.3, and observe the display unit for the patterns shown in Figures 5-2 through 5-8 at the various switch register settings. If the patterns are distorted, the potentiometers specified should be adjusted until they approximate the idealized patterns shown.

NOTE

When the equipment is initially installed, all potentiometers should be set to mid-range.

5.6.1 Preliminary Instructions

Control Switch Settings

The control switch settings for the various tests are given in Tables 5-1 through 5-3.

NOTE

Place the analog function generator on Module Extender W983 for access to 1-turn potentiometers, if adjustment of these potentiometers is required. Unless otherwise noted, the locations of the potentiometers cited in the following procedures are shown in Figures 5-9 and 5-10. The display patterns are shown optimized in Figures 5-2 through 5-8.

5.6.2 Test and Adjustment

Analog Function Generator and Timing Generator

To initially adjust or to verify the current adjustment settings of the Analog Function Generator and Timing Generator potentiometers, the following procedures should be used. In these procedures two dots are displayed on the screen. One dot will remain stationary, while the other will move in response to adjustments made on the potentiometers. The vector formed by the two dots represents the error vector and indicates the relative adjustment necessary on the X and Y potentiometer. This error vector is to be decreased to zero (both dots merging).

NOTE

The octal number appearing in Switch Register 2 to 11 (do not disturb the control 0 and 1 settings) is proportional to the delay time between dot displays, with Switch Register 11 the least significant bit. On very fast repetition rates, a *tail* may appear on the display. This is normal and is to be ignored.

X and Y Sample and Hold Drift Rates – To check the X and Y sample and hold drift rates perform the following:

a. Start the program at location 2600 with Switch Register = 2000.

b. Set the VT01 INTENSITY and OPERATING LEVEL controls (behind front panel access door) to mid range.

c. Adjust X Sample and Hold Drift Rate (R8) and Y Sample and Hold Drift Rate (R39) until only one point is seen on the screen.

d. Increase the number in Switch Register 5 to 11 for a longer delay and readjust if necessary until there is only one point ± 1 dot when Switch Register equals 100_8.

e. Erase the screen with the ERASE switch on the VT01 as required to clean up the trace.

Integrator Drift Rate – To check the integrator drift rate perform the following:

a. Start the program at location 2600 with Switch Register = 6000.

b. Two dots should appear on the screen. If they appear as lines instead, adjust the X and Y sample and hold zero (R1 and R32) pots until the lines become dots.

c. Adjust X Integrator Drift Rate (R17) and Y Integrator Drift Rate (R50) until only one point is seen on the screen.

d. Increase the number in Switch Register 5 to 11 for a longer delay and readjust if necessary until there is only one point ± 1 dot size when Switch Register equals 100_8.

Adjustment of X and Y Sample and Hold Zeros and Circle Mode Zeros – (It will be necessary to place the A312 module on an extender card if readjustment is required.) Turn the VT01 OPERATING LEVEL control fully counterclockwise. When performing initial adjustment only, remove left side of cover of VT01 and turn both gain potentiometers (R45 and R145, Figure 5-13 of 611 Manual) fully counterclockwise, and turn the two centering potentiometers (R44 and R144 at bottom right of Figure 5-10 in 611 Manual) to their middle position . Put the two slide switches (SW204 and SW202) at upper right to their center position, if not previously accomplished. The control Switch Register settings for the following tests are summarized in the Table 5-3. The function of the four potentiometer adjustments relative to the pattern of Figure 5-2 are given in Table 5-5.

Start the program at location 3000 with Switch Register = 0001 and perform the following:

a. Adjust X Sample and Hold Zero (R1) and/or Y Sample and Hold Zero (R32) so that all corners meet ± 1 coordinate (.02 inches).

b. Adjust X Circle Mode Zero (R44) for circle to be centered along the Y axis.

c. Adjust Y Circle Mode Zero (R63) until the circle becomes a dot. It should have a maximum diameter of 2 with the center just showing a non-stored opening, as shown in Figure 5-2.

Adjustments of Circle Mode Rates – The function of the two potentiometers, Circle Mode Rate 1 (R24) and Circle Mode Rate 2 (R62) is to make the pattern, shown in Figure 5-3, a circle rather than an elipse.

Start program at location 3000 Switch Register = 0002 and perform the following:

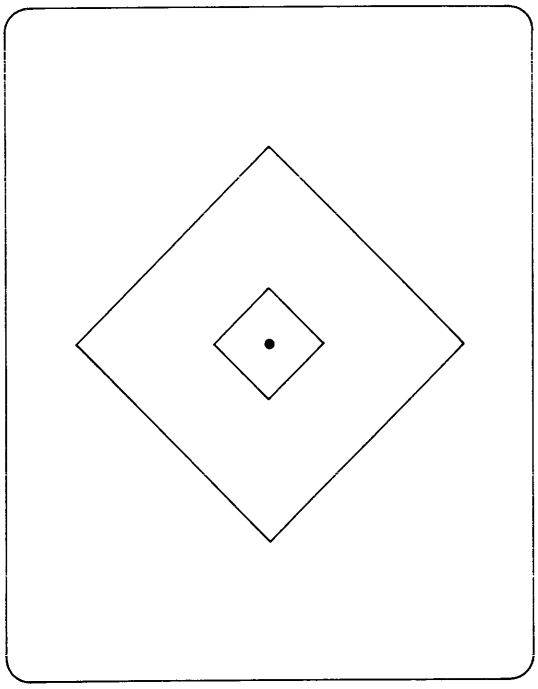


Figure 5-2. Circle Mode Zero and X and Y Sample/ Hold Zero, Adjustment Display Pattern

a. Adjust Rate 1 (R24) and Rate 2 (R62) until the circle is an equal distance from all four calibration lines.

b. Adjust Rate 1 and Rate 2 in opposite directions until the circle closes and all four calibration lines touch the edge of the circle, as shown in Figure 5-3.

NOTE

It may be necessary to retouch X Sample and Hold (R1) and Y Sample and Hold (R32) to obtain an exact crossing of the four calibration lines at the center.

Adjustment of the Stroke Timing Generator – The function of the potentiometer (R7) on M712 is to adjust the timing used to genreate arcs correctly as shown in pattern Figure 5-4.

Start the program at location 3000 Switch Register = 0004 and adjust potentiometer (R7) on M712 until the arc just meets the top of the Y axis calibration line.

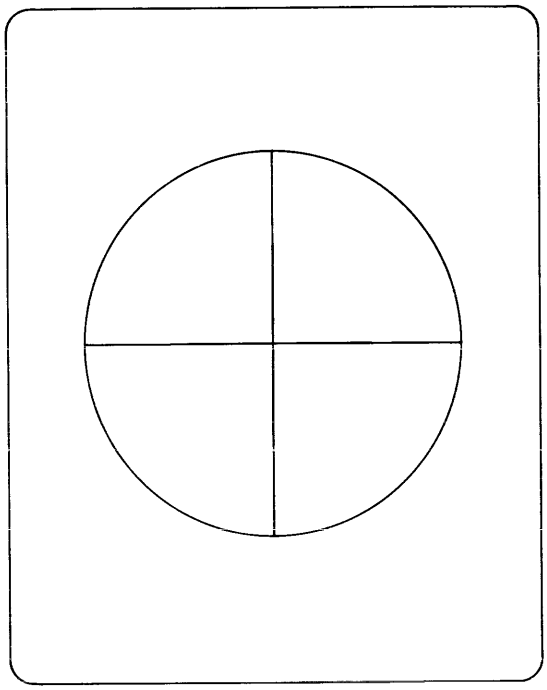


Figure 5-3. Circle Mode Rate, Adjustment Display Pattern

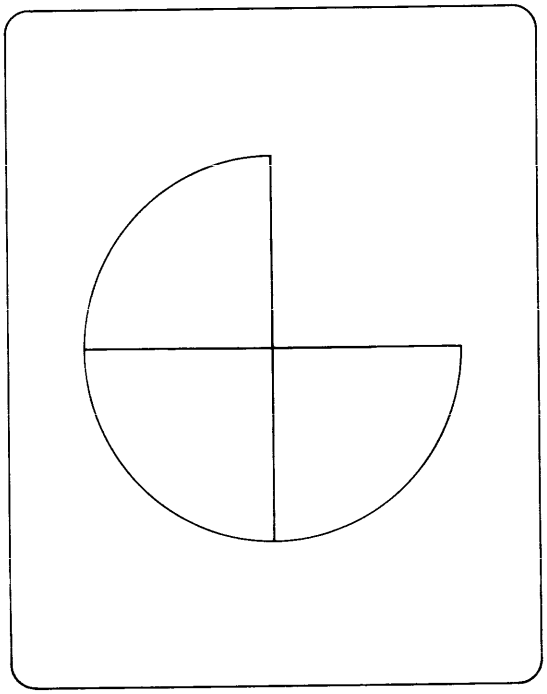


Figure 5-4. Stroke Timing Generator, Adjustment Display Pattern

Adjustment of X and Y Absolute Zero and Absolute Gains – The function of the four potentiometer adjustments relative to the pattern of Figure 5-5 are given in Table 5-6.

Start the program at location 3000 Switch Register = 0010 and perform the following:

a. Adjust X Absolute Zero (R10) and Y Absolute Zero (R41) until the dot in the middle of the cross is minimum size.

b. Adjust X Absolute Gain (R20) until the two vertical lines are parallel and the upper left-hand and lower right-hand corners close.

c. Adjust Y Absolute Gain (R52) until the opposite two corners close. All four should be closed, if not, it may be necessary to retouch X Absolute Gain (R20).

Adjustment of X and Y Circle Mode Center Gains – The function of the two potentiometers, X CM Center Gain (R15), and Y CM Center Gain (R40), is to minimize the size of the three circles to three dots as shown in Figure 5-6. They are actually circles with zero radius.

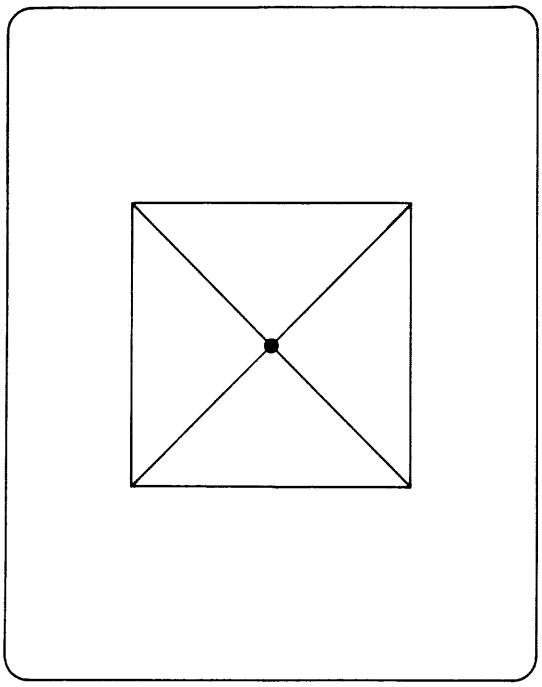


Figure 5-5. Absolute Vector, Adjustment Display Pattern

Start the program at location 3000 Switch Register = 0020 and perform the following:

a. Adjust X CM Center Gain (R15) until the circle at the right is a dot.

b. Adjust Y CM Center Gain (R40) until the circle at the top is a dot.

NOTE

It may be necessary to slightly retouch the settings on X Circle Mode Zero (R44) to get a perfect dot at the top, Y Circle Mode Zero (R63) to get a perfect dot at the right, and X Absolute Zero (R10) and Y Absolute Zero (R41) to get a perfect dot at the bottom left.

Adjustment of X and Y Point Mode Zeros and Gains – The function of the four potentiometer adjustments relative to the pattern of Figure 5-7 are given in Table 5-7.

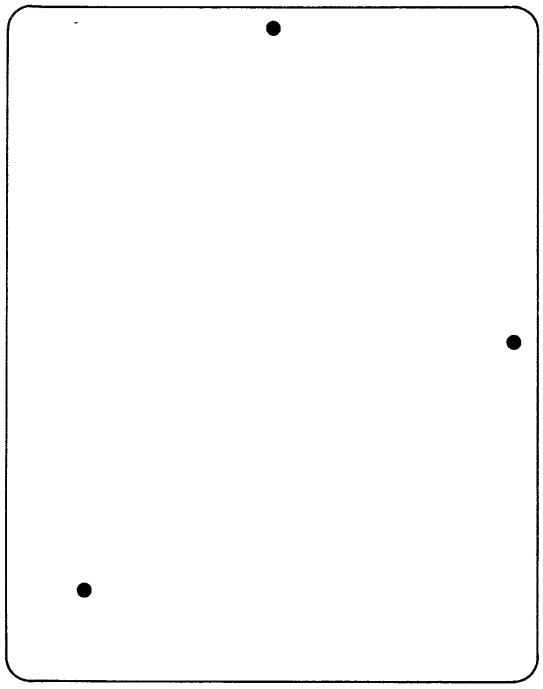


Figure 5-6. Circle Mode Center Gain, Adjustment Display Pattern

Start the program at location 3000 with Switch Register = 0040 and perform the following:

a. Adjust X Point Mode Zero (R27) so that the dots are an equal distance from the two outside vertical lines and the center dot falls on the center cross line.

b. Adjust Y Point Mode Zero (R58) so that the dots are an equal distance from the two outside horizontal lines and the center dot falls on the center cross lines.

c. Adjust X Point Mode Gain (R26) so that the vertical dots fall along the two vertical outside lines.

d. Adjust Y Point Mode Gain (R55) so that the horizontal dots fall along the two horizontal outside lines.

NOTE

The four dots appearing outside the box pattern will be used later to align VT01 gain and positioning potentiometers.

Adjustment of X and Y Short Vector Gains – The function of the two potentiometer adjustments relative to the pattern of Figure 5-8 are given in Table 5-8.

Start program at location 3000 with Switch Register = 0100 and perform the following:

a. Adjust X Short Vector Gain (R13) until the two horizontal lines are equal.

b. Adjust Y Short Vector Gain (R48) until the two vertical lines are equal.

NOTE

Ignore any slight skew which may be present in this pattern.

Composite Picture – A composite picture of all adjustments may be obtained by setting Switch Register to 0177.

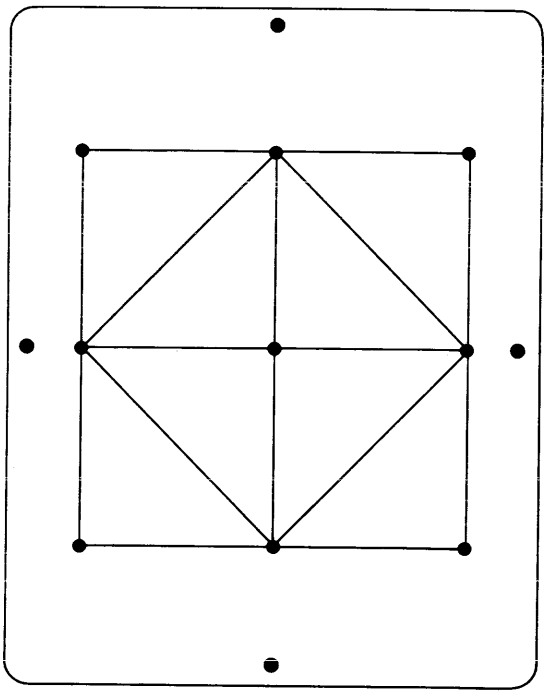


Figure 5-7. Point Mode Zero, Adjustment Display Pattern

Adjustment of VT01 Gain and Centerings – This step centers the pattern and sets the correct scope gain. (Refer to 611 Manual Figures 5-13 and 5-10 for potentiometer locations.)

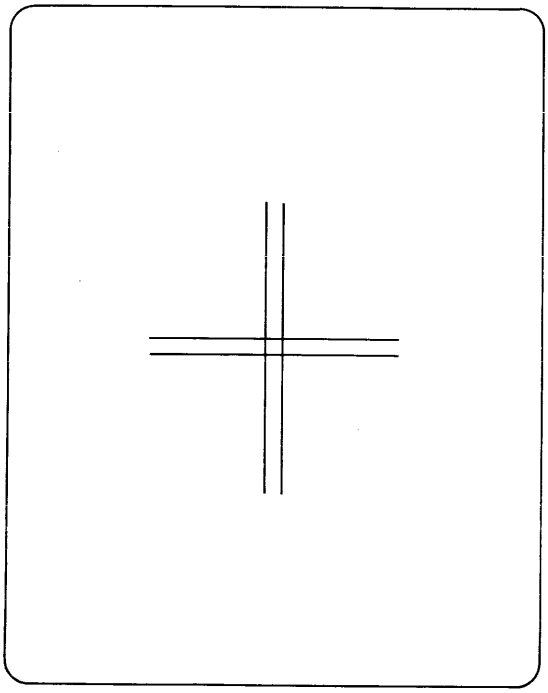


Figure 5-8. Short Vector Gain, Adjustment Display Pattern

Start the program at location 3000 with Switch Register = 0040 and perform the following:

a. Adjust the gain and centering potentiometers (R44, R45, R144 and R145 of the VT01) until the four outside dots of Figure 5-7 just contact the edge of the storage tube visible area.

b. Replace the left side cover of the VT01.

Adjustment of VT01 Display Characteristics – Push the VT01 TEST SPIRAL switch (red button at bottom of front panel controls behind access door) and hold it in until a spiral pattern appears on the screen. Adjust the INTENSITY control to approximately two thirds full range (clockwise) and then adjust the OPERATING LEVEL control until the stored image remains stored and neither bleeds up (blots) or drops out (decays). This will place the OPERATING LEVEL control about mid range. Then decrease the INTENSITY control until the spiral just begins not to be stored on the outer loop.

Adjustment of Joystick Balance Potentiometers and Checking of Cursor Interrupt Flag – Turn the VT01 controls as follows:

OPERATING LEVEL – mid range

INTENSITY – mid range

WRITE-THRU INTENSITY – fully counterclockwise

Start the program at location 2000. A horizontal and vertical axis should be plotted on the CRT. Center the Joystick and turn the WRITE-THRU INTENSITY control of the VT01 until the current position of the *Joystick* begins to show on the screen. If not, move it until it does. The correct setting for WRITE-THRU INTENSITY control produces a visible elliptical pointer which does not remain stored (except at very edges of screen). Adjust the Balance Pots in the joystick hardware so that the cursor circle is at the origin (center when the *Joystick* is vertical and the full limits of the screen may be reached in plus and minus X and Y. This may require mechanical adjustment of the *main* potentiometers in the *joystick* hardware. Depress the *cursor interrupt button*. The teleprinter should ring. If it does not, the computer will halt if an error occurred. If the computer did not stop (and the bell didn't ring), the computer never saw the cursor interrupt. Check that portion of the control logic circuitry for malfunctions.

Adjustment of X and Y Comparator Zeros, X and Y Comparator Gains – Start the program at location 2200. A horizontal and vertical axis should be plotted on the CRT. The current position of the *Joystick* should also show on the screen and a point which will move with the *cursor*.

Move the cursor to the origin (center) and adjust X Comparator Zero (R93) and Y Comparator Zero (R83) until the point falls in the center of the cursor circle. These adjustment controls are located on the A612 D/A Board. Move the cursor to the farthest point on the X axis and adjust X Comparator Gain (R86) until the point falls in the center of the circle. Move the cursor to the farthest point on the Y axis and adjust Y Comparator Gain (R88) until the point falls in the center of the circle. Slowly move the cursor circle around the screen, the point should stay in the circle at all points on the screen. If not, readjust the appropriate potentiometer until it does.

Visual Verification of Digital to Analog Circuitry, Analog Comparator, and Relative Worth of X and Y Sample and Hold and Integrator Circuits – Start the program at location 1600. Set Switch Register 0 and 1 to the settings in Table 5-10 for unit to be tested. Switch Register 2 to 11 for value to be output to unit under test.

The reference value sent to the selected unit will appear as returned on the accumulator indicator lights. This should agree within 4 counts of the reference value.

Visual Verification of Stroke Vector Character Generator – Start the program at location 2400. Type characters on the TTY keyboard. The characters should appear on the display unit and the image should be legible and well formed. If excessive distortion or noise is present, the

characters may be viewed in the refreshed mode by raising Switch Register bit 0. The code in the Switch Register, bits 6 through 11, will be the refreshed character code.

NOTE

The typing can be returned to the top left by using the control K key.

CAUTION

The writing intensity may have to be lowered to prevent possible damage to the phosphor of the screen in the refreshed mode.

The refreshed patterns provide convenient test signals which can be synchronized using AB(1).

Error Diagnosis of Program Diagnosible Errors

Start the Program at Location 0200 – The program will test the basic IOT set (except cursor IOT's), D to A Network and Comparator, X and Y Sample and Hold and Integrator drift rates; and then the reset signal zeros the Sample and Hold and Integrator Circuits. Teleprinter bell will ring after each pass through all tests.

Start the Program at 0200 – Depress *cursor interrupt button* repeatedly. The bell should ring on the teleprinter each time the button is depressed. If the computer stops, an error has occurred. If the bell is not rung, the program does not see the *cursor interrupt flag.*

5.7 REPAIR AND REPLACEMENT

Repair and replacement of repair parts of KV Controller require no special instructions. Refer to the parts location diagrams and repair parts lists of chapter 6 for parts replacement.

TABLE 5-1. X OR Y SAMPLE AND HOLD OR INTEGRATOR CALIBRATION TESTS

Switch Register		Test
0	0	X Sample and Hold
0	1	X Integrator
1	0	Y Sample and Hold
1	1	Y Integrator

Switch Register 2 to 11 -D/A value to be sent to circuit

TABLE 5-2. X AND Y SAMPLE AND HOLD AND INTEGRATOR DRIFT RATE ADJUST ROUTINES USING RESET AND THE CRT

Switch Register	Setting	Test
0	0	Sample and Hold Drift Rates
	1	Integrator Drift Rates
1	0	Do Not Issue *Reset*
	1	Issue *Reset*

Switch Register 2 to 11 - Delay between plots

TABLE 5-3. ANALOG FUNCTION GENERATOR AND TIMING GENERATOR ADJUSTMENT ROUTINES

Switch Register	Setting	Test
0	1	Force Short Vector (Write thru)
5	1	Short Vector Gains
6	1	Point Mode Zeros, Point Mode Gains
7	1	Circle Mode Gains
8	1	Absolute Zeros, Absolute Gains
9	1	Stroke Timing Generator
10	1	Circle Mode Rates
11	1	Sample and Hold Zeros, Circle Mode Zeros

TABLE 5-4. STARTING ADDRESSES

Address	Routine or Test
0200	IOT Tests, D to A Test, Comparator Test, Sample and Hold and Integrator Drift Rate Tests, Reset Tests
1000	X or Y Sample and Hold or Integrator Calibration Tests
2000	*Joystick* balance potentiometers adjust and cursor interrupt test routines
2200	X and Y Comparator Gains and Comparator Zeros Adjust Routine
2400	Character generator exercisor (for determining sources of analog noise)
2600	X and Y Sample and Hold and Integrator drift rate adjust routines using *Reset* and the CRT
3000	Analog Function Generator and Timing Generator Adjustment Routines

TABLE 5-5. FUNCTION OF GAIN AND CENTERING POTENTIOMETERS

Potentiometer	Function
X Sample & Hold Zero (R1)	Displaces the pattern along the X axis.
Y Sample & Hold Zero (R32)	Displaces the pattern along the Y axis.
X Circle Mode Zero (R44)	The circle inside the smaller triangle will open up along the X axis.
Y Circle Mode Zero (R63)	The circle inside the smaller triangle will open up along the Y axis.

TABLE 5-6. FUNCTION OF X AND Y ABSOLUTE ZERO AND ABSOLUTE GAIN POTENTIOMETER

Potentiometer	Function
X Absolute Zero (R10)	Displaces the dot in the middle of the cross line along the X axis.
Y Absolute Zero (R41)	Displaces the dot in the middle of the cross lines along the Y axis.

TABLE 5-6. FUNCTION OF X AND Y ABSOLUTE ZERO AND ABSOLUTE GAIN POTENTIOMETER (cont)

Potentiometer	Function
X Absolute Gain (R20)	Displaces the pattern along the X axis.
Y Absolute Gain (R52)	Displaces the pattern along the Y axis.

TABLE 5-7. FUNCTION OF X AND Y POINT MODE ZERO AND GAIN POTENTIOMETERS

Potentiometer	Function
X Point Mode Zero (R27)	Moves only the dots along the X axis.
Y Point Mode Zero (R58)	Moves only the dots along the Y axis.
X Point Mode Gain (R26)	Increases or decreases the distance between the dots on the X axis only.
Y Point Mode Gain (R55)	Increases or decreases the distance between the dots on the Y axis only.

TABLE 5-8. FUNCTION OF X AND Y SHORT VECTOR GAIN POTENTIOMETERS

Potentiometer	Function
X Short Vector Gain (R13)	Moves only one of the horizontal lines along the X axis.
Y Short Vector Gain (R48)	Moves only one of the vertical lines along the Y axis.

TABLE 5-9. FUNCTION OF GAIN AND CENTERING POTENTIOMETERS

Potentiometer	Function
R45	Adjust X gain on VT01.
R145	Adjusts Y gain on VT01.
R44	Adjust X centering on VT01.
R144	Adjusts Y centering on VT01.

TABLE 5-10. SWITCH POSITIONS FOR VISUAL CHECK

Unit	Switch Register 0	Switch Register 1
X Sample and Hold	0	0
X Integrator	0	1
Y Sample and Hold	1	0
Y Integrator	1	1

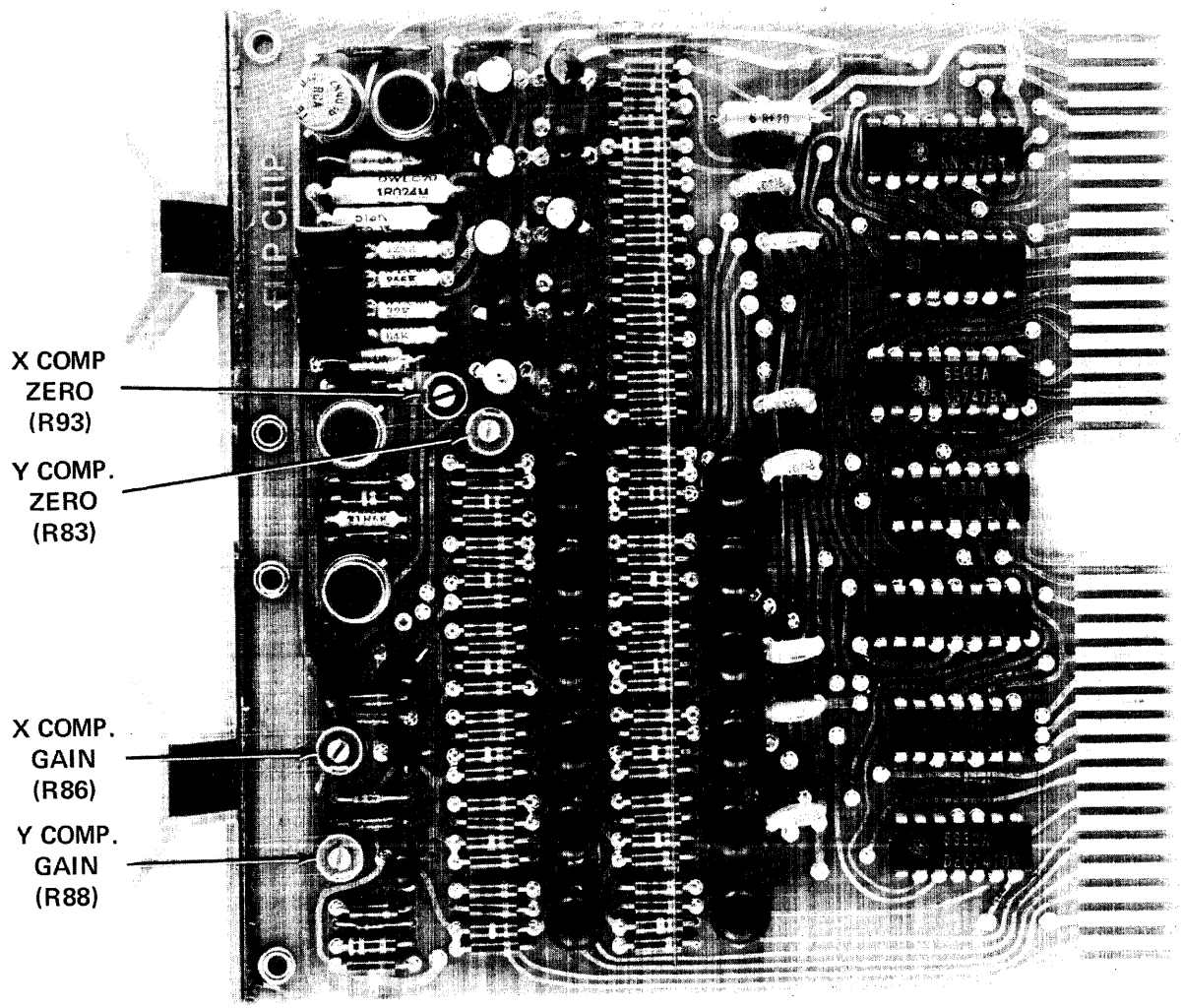


Figure 5-9. Digital-to-Analog Converter and Gate Logic Module A612, Adjustable Parts Location Diagram

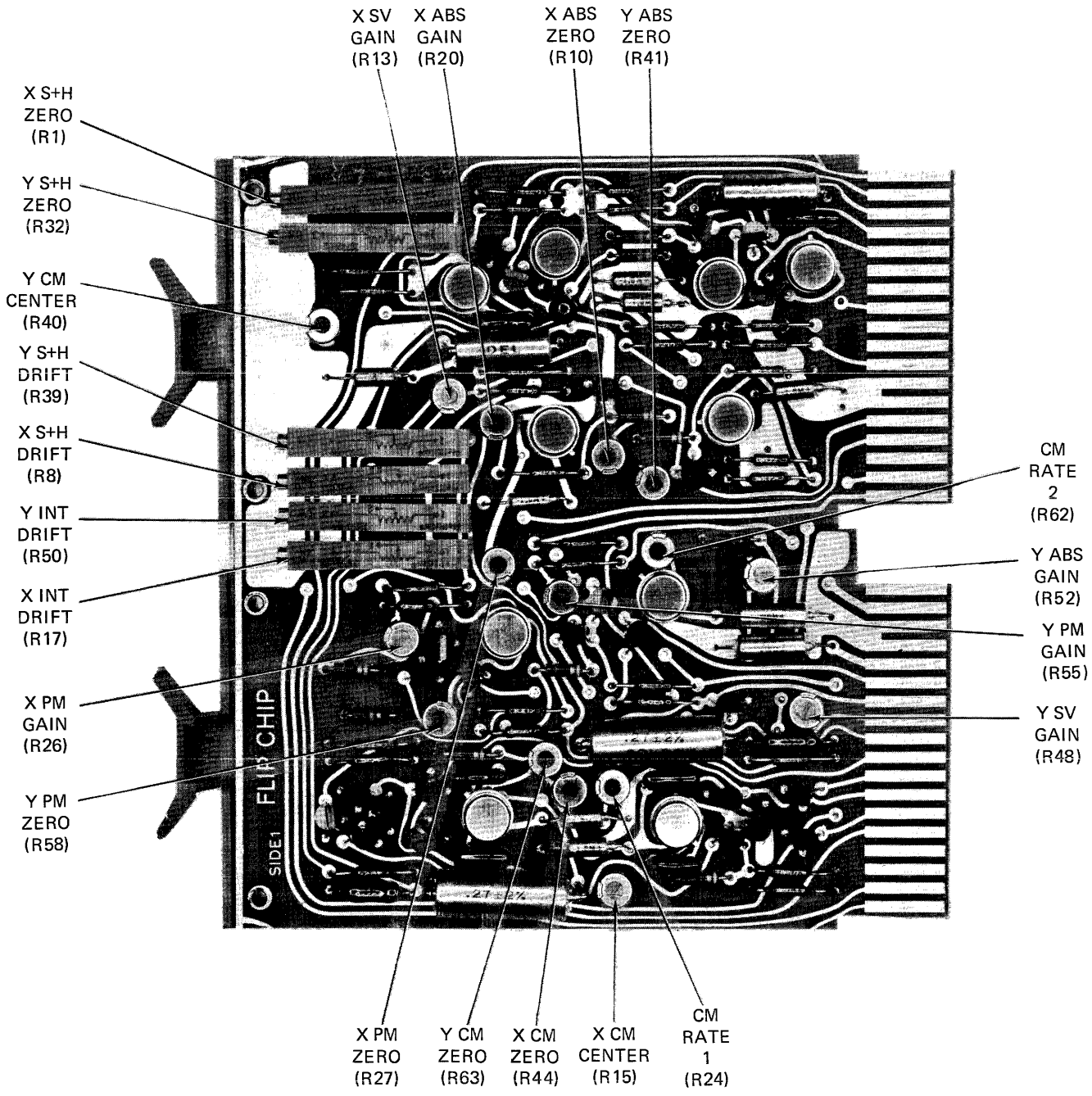


Figure 5-10. Analog Function Generator Module A312, Adjustable Parts Location Diagram

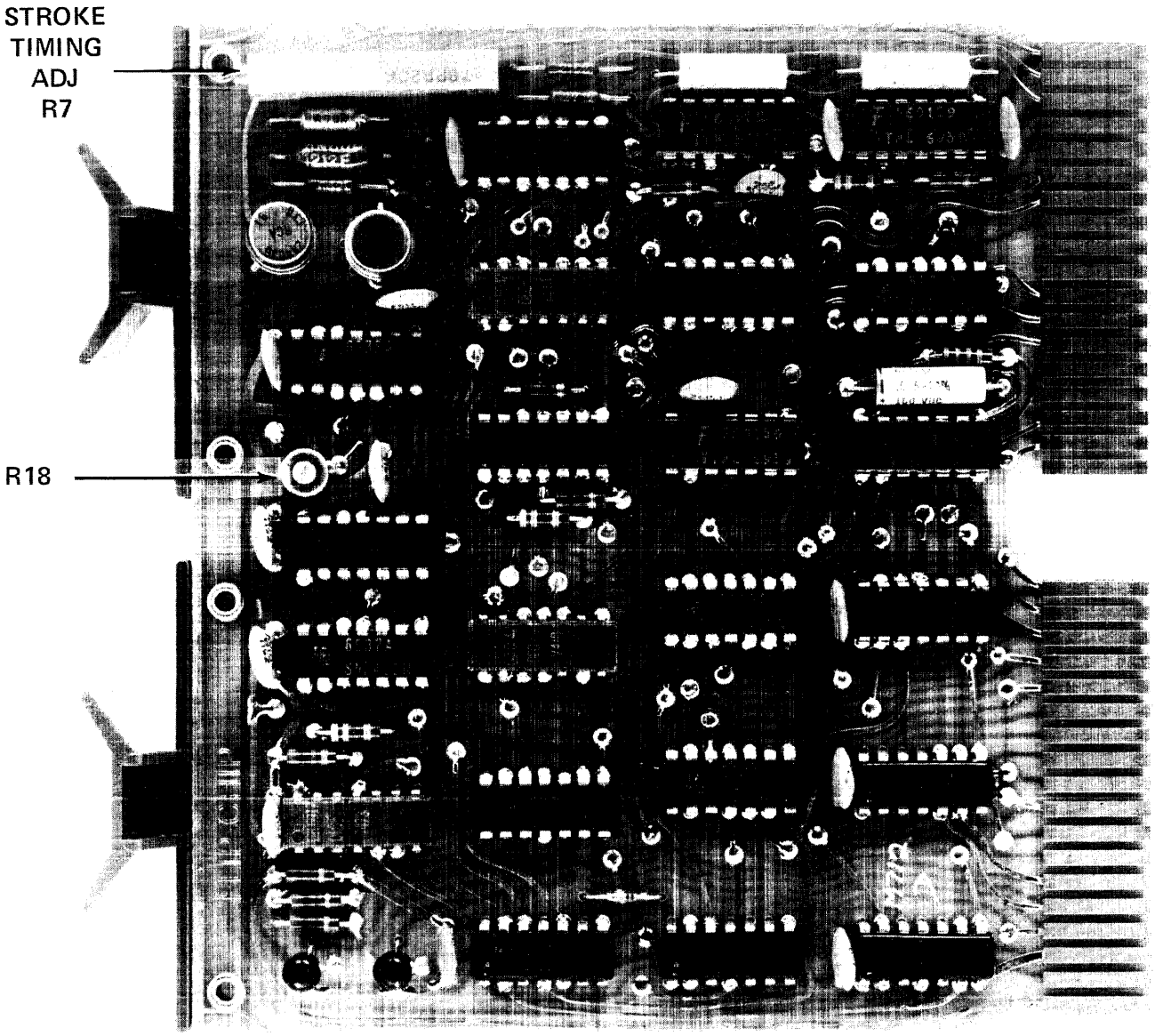


Figure 5-11. Timing Generator Module M712, Adjustable Parts Location Diagram

CHAPTER 6
REPAIR PARTS LISTS

This chapter lists the replaceable parts of the modules of the KV Controller. The parts are listed in alphanumerical order according to reference designation. Pertinent data, such as, DEC stock number and manufacturer's type or part, number or both and descriptions, are provided for each part. Table 6-1 is a cross reference list for location of the parts list and the associated schematic diagram and parts location diagram for each module of the controller. Repair parts lists for optional modules and equipment are not provided. For repair parts data of optional equipment, refer to the applicable instruction manual listed in the Related Documents paragraph of the Introduction.

NOTE: Unless otherwise specified:
1. Resistors are expressed in ohms, 1/4 Watt, ±5%.
2. Capacitors are expressed in microfarads.

TABLE 6-1. REPAIR PARTS DATA CROSS REFERENCE LIST

Name	Module Type	Parts List (Table)	Parts Location Diagram (Figure)	Schematic Diagram (Figure)
Timing Generator	M712	6-2	6-1	7-1
Digital-to-Analog Converter and Gate Logic	A612	6-3	6-2	7-2
Analog Function Generator	A312	6-4	6-3	7-3
Voltage Regulator	A712	6-5	6-4	7-4

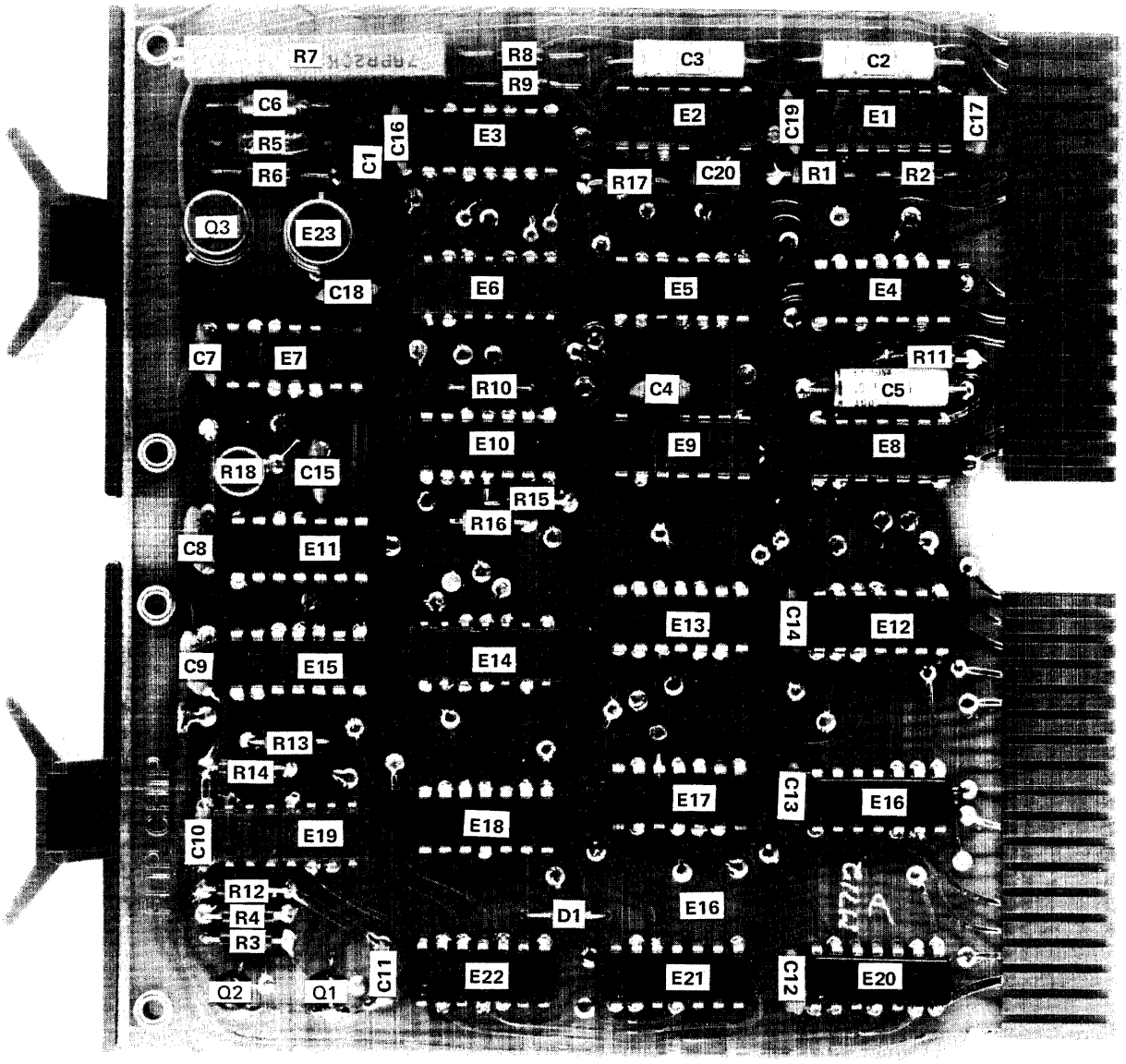


Figure 6-1. Timing Generator Module M712, Parts Location Diagram

TABLE 6-2. TIMING GENERATOR MODULE, M712 REPAIR PARTS LIST

Ref Desig	DEC. Stock No.	MFR. Type or Part No.	Description
C1	10-00011		CAPACITOR, 47 pfd
C2 and C3	10-02630		CAPACITOR, MYLAR, 0.015
C4	10-00055		CAPACITOR, 0.0022
C5	10-02630		CAPACITOR, MYLAR, 0.015
C6	10-01776		CAPACITOR, 1.0
C7 thru C19	10-01610		CAPACITOR, 0.01
C20	10-00043		CAPACITOR, .001
E1	19-09487	9601 (Fairchild)	INTEGRATED CIRCUIT
E2	19-09487	9601 (Fairchild)	INTEGRATED CIRCUIT
E3	19-05547	SN7474N (Texas Instrument)	INTEGRATED CIRCUIT
E4	19-09004	SN7402 (Texas Instrument)	INTEGRATED CIRCUIT
E5	19-05575	SN7400 (Texas Instrument)	INTEGRATED CIRCUIT
E6	19-05576	SN7410 (Texas Instrument)	INTEGRATED CIRCUIT
E7	19-05575	SN7400 (Texas Instrument)	INTEGRATED CIRCUIT
E8	19-09487	9601 (Fairchild)	INTEGRATED CIRCUIT
E9	19-09487	9601 (Fairchild)	INTEGRATED CIRCUIT
E10	19-05547	SN7474 (Texas Instrument)	INTEGRATED CIRCUIT
E11	19-09054	SN7493 (Texas Instrument)	INTEGRATED CIRCUIT
E12	19-05575	SN7400 (Texas Instrument)	INTEGRATED CIRCUIT
E13	19-09004	SN7402 (Texas Instrument)	INTEGRATED CIRCUIT
E14	19-05576	SN7410 (Texas Instrument)	INTEGRATED CIRCUIT
E15	19-09004	SN7402 (Texas Instrument)	INTEGRATED CIRCUIT
E16	19-05577	SN7420 (Texas Instrument)	INTEGRATED CIRCUIT
E17	19-05575	SN7400 (Texas Instrument)	INTEGRATED CIRCUIT
E18	19-05575	SN7400 (Texas Instrument)	INTEGRATED CIRCUIT
E19	19-05587	SN7473 (Texas Instrument)	INTEGRATED CIRCUIT
E20 thru E22	19-05577	SN7420 (Texas Instrument)	INTEGRATED CIRCUIT
E23	19-09371	LM300	INTEGRATED CIRCUIT

TABLE 6-2. TIMING GENERATOR MODULE, M712 REPAIR PARTS LIST (cont)

Ref Desig	DEC. Stock No.	MFR. Type or Part No.	Description
Q1 and Q2	15-05302	2N4274	TRANSISTOR
Q3	15-09390	2N4036 (RCA)	TRANSISTOR
R1	13-00295		RESISTOR, fxd, 330
R2	13-01401		RESISTOR, fxd, 750
R3 and R4	13-00365		RESISTOR, fxd, .1K
R5	13-03313		RESISTOR, fxd, 12.1K, ± 1%, 1/8w
R6	13-05128		RESISTOR, fxd, 5.62K, ± 1%, 1/8w
R7	13-09409	Type 78 PR (Helitrim)	POTENTIOMETER, 15 turns, 20K
R8	13-03155		RESISTOR, fxd, 21.5K, ± 1%, 1/8w
R9	13-09417		RESISTOR, fxd, 27.4K, ± 1%, 1/8w
R10 and R11	13-00510		RESISTOR, fxd, 33K, ± 10%, 1/4w
R12	13-02388		RESISTOR, fxd, 2K
R13	13-00295		RESISTOR, fxd, 330
R14 and R15	13-01401		RESISTOR, fxd, 750
R16	13-00295		RESISTOR, fxd, 330K
R16	13-00295		RESISTOR, fxd, 330
R17	13-00250		RESISTOR, fxd, 150
R18	13-09150-06	Type 62 PR (Helitrim)	POTENTIOMETER, 50K

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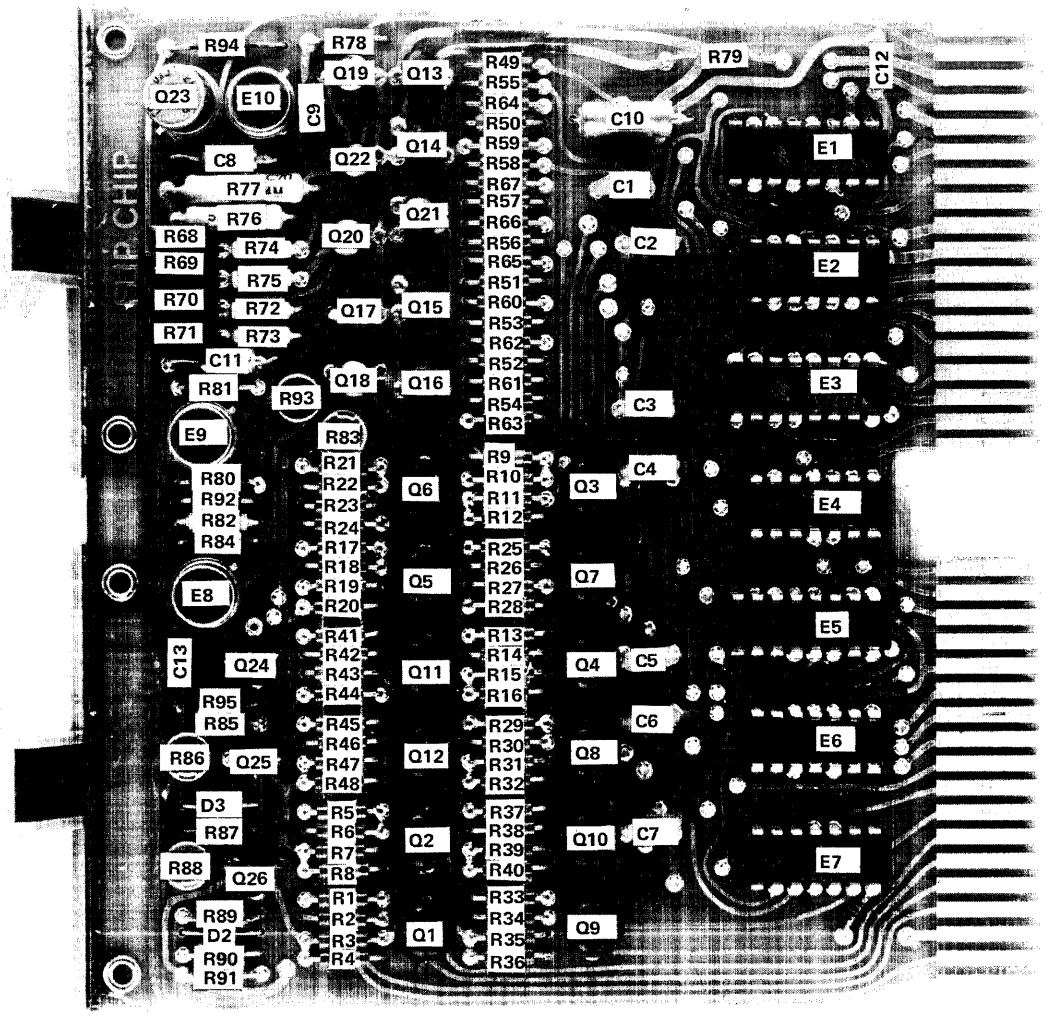


Figure 6-2. Digital-to-Analog Converter and Gate Logic Module A612, Parts Location Diagram

TABLE 6-3. DIGITAL-TO-ANALOG CONVERTER AND GATE LOGIC MODULE A612, REPAIR PARTS LIST

Ref Desig	DEC. Stock No.	MFR. Type or Part No.	Description
C1 thru C7, C12	10-01610		CAPACITOR, 0.01
C8, C11	10-01776		CAPACITOR, 1
C9	10-00079		CAPACITOR, 47 pf
C10	10-00067		CAPACITOR, 6.8
D1	11-00123	IN750	SEMICONDUCTOR DEVICE
D2	11-00114	D664	SEMICONDUCTOR DEVICE
D3	11-00114	D664	SEMICONDUCTOR DEVICE
E1	19-09050	SN7475N (Texas Instrument)	INTEGRATED CIRCUIT
E2	19-05575	SN7400N (Texas Instrument)	INTEGRATED CIRCUIT
E3	19-09050	SN7475N (Texas Instrument)	INTEGRATED CIRCUIT
E4	19-05575	SN7400N (Texas Instrument)	INTEGRATED CIRCUIT
E5	19-09050	SN7475N (Texas Instrument)	INTEGRATED CIRCUIT
E6	19-05576	SN7410N (Texas Instrument)	INTEGRATED CIRCUIT
E7	19-05576	SN7410N (Texas Instrument)	INTEGRATED CIRCUIT
E8	19-09498	LM301A (Motorola)	OPERATIONAL AMPLIFIER
E9	19-09499	LM307 (Motorola)	OPERATIONAL AMPLIFIER
E10	19-09371	LM307 (Motorola)	VOLTAGE REGULATOR
Q1 thru Q12	15-02979	2N3638	TRANSISTOR
Q13 thru Q17*	15-03097		TRANSISTOR
Q18 thru Q22*	15-03097		TRANSISTOR
Q22			TRANSISTOR
Q23	15-09390	2N4036	TRANSISTOR
Q24 and Q25	15-09374	2N5459	TRANSISTOR, FET
Q26	15-05302	2N4274	TRANSISTOR
R1	13-00365		RESISTOR, fxd, 1K, ±5%, 1/4w
R2	13-02388		RESISTOR, fxd, 2K, ±5%, 1/4w
R3	13-00496		RESISTOR, fxd, 15K, ±5%, 1/4w
R4	13-00426		RESISTOR, fxd, 2.7K, ±5%, 1/4w
R5	13-00365		RESISTOR, fxd, 1K, ±5%, 1/4w
R6	13-02388		RESISTOR, fxd, 2K, ±5%, 1/4w
R7	13-00496		RESISTOR, fxd, 15K, ±5%, 1/4w
R8	13-00426		RESISTOR, fxd, 2.7K, ±5%, 1/4w
R9	13-00365		RESISTOR, fxd, 1K, ±5%, 1/4w

TABLE 6-3. DIGITAL-TO-ANALOG CONVERTER AND GATE LOGIC MODULE A612, REPAIR PARTS LIST (cont)

Ref Desig	DEC. Stock No.	MFR. Type or Part No.	Description
R10	13-02388		RESISTOR, fxd, 2K, ±5%, 1/4w
R11	13-00496		RESISTOR, fxd, 15K, ±5%, 1/4w
R12	13-00426		RESISTOR, fxd, 2.7K, ±5%, 1/4w
R13	13-00365		RESISTOR, fxd, 1K, ±5%, 1/4w
R14	13-02388		RESISTOR, fxd, 2K, ±5%, 1/4w
R15	13-00496		RESISTOR, fxd, 15K, ±5%, 1/4w
R16	13-00426		RESISTOR, fxd, 2.7K, ±5%, 1/4w
R17	13-00365		RESISTOR, fxd, 1K, ±5%, 1/4w
R18	13-02388		RESISTOR, fxd, 2K, ±5%, 1/4w
R19	13-00496		RESISTOR, fxd, 15K, ±5%, 1/4w
R20	13-00426		RESISTOR, fxd, 2.7K, ±5%, 1/4w
R21	13-00365		RESISTOR, fxd, 1K, ±5%, 1/4w
R22	13-02388		RESISTOR, fxd, 2K, ±5%, 1/4w
R23	13-00496		RESISTOR, fxd, 15K, ±5%, 1/4w
R24	13-00426		RESISTOR, fxd, 2.7K, ±5%, 1/4w
R25	13-00365		RESISTOR, fxd, 1K, ±5%, 1/4w
R26	13-02388		RESISTOR, fxd, 2K, ±5%, 1/4w
R27	13-00496		RESISTOR, fxd, 15K, ±5%, 1/4w
R28	13-00426		RESISTOR, fxd, 2.7K, ±5%, 1/4w
R29	13-00365		RESISTOR, fxd, 1K, ±5%, 1/4w
R30	13-02388		RESISTOR, fxd, 2K, ±5%, 1/4w
R31	13-00496		RESISTOR, fxd, 15K, ±5%, 1/4w
R32	13-00426		RESISTOR, fxd, 2.7K, ±5%, 1/4w
R33	13-00365		RESISTOR, fxd, 1K, ±5%, 1/4w
R34	13-02388		RESISTOR, fxd, 2K, ±5%, 1/4w
R35	13-00496		RESISTOR, fxd, 15K, ±5%, 1/4w
R36	13-00426		RESISTOR, fxd, 2.7K, ±5%, 1/4w
R37	13-00365		RESISTOR, fxd, 1K, ±5%, 1/4w
R38	13-02388		RESISTOR, fxd, 2K, ±5%, 1/4w
R39	13-00496		RESISTOR, fxd, 15K, ±5%, 1/4w
R40	13-00426		RESISTOR, fxd, 2.7K, ±5%, 1/4w
R41	13-00365		RESISTOR, fxd, 1K, ±5%, 1/4w
R42	13-02388		RESISTOR, fxd, 2K, ±5%, 1/4w
R43	13-00496		RESISTOR, fxd, 15K, ±5%, 1/4w
R44	13-00426		RESISTOR, fxd, 2.7K, ±5%, 1/4w
R45	13-00365		RESISTOR, fxd, 1K, ±5%, 1/4w
R46	13-02388		RESISTOR, fxd, 2K, ±5%, 1/4w
R47	13-00496		RESISTOR, fxd, 15K, ±5%, 1/4w
R48	13-00426		RESISTOR, fxd, 2.7K, ±5%, 1/4w
R49 thru R58	13-01320		RESISTOR, fxd, 1.2K, ±5%, 1/4w
R59	13-00444		RESISTOR, fxd, 3.9K, ±5%, 1/4w
R60	13-00426		RESISTOR, fxd, 2.7K, ±5%, 1/4w
R61	13-00417		RESISTOR, fxd, 2.2K, ±5%, 1/4w
R62 thru R67	13-02388		RESISTOR, fxd, 2K, ±5%, 1/4w
R69	13-05511		RESISTOR, fxd, 4K ±0.01%, .3w
R70	13-05512		RESISTOR, fxd, 8K, ±0.01%, .3w
R71	13-05513		RESISTOR, fxd, 16K, ± .01%, .3w
R72	13-05514		RESISTOR, fxd, 32K, ± .1%, 1/8w
R73	13-05516		RESISTOR, fxd, 64K, ± .1%, 1/8w
R68	13-05510		RESISTOR, fxd, .2K ±.01%, .3w

TABLE 6-3. DIGITAL-TO-ANALOG CONVERTER AND GATE LOGIC MODULE A612, REPAIR PARTS LIST (cont)

Ref Desig	DEC. Stock No.	MFR. Type or Part No.	Description
R74	13-05517		RESISTOR, fxd, 128K, ±.1%, 1/8w
R75	13-05518		RESISTOR, fxd, 256K, ±.1%, 1/8w
R76	13-05519		RESISTOR, fxd, 512K, ±1%, 1/4w
R77	13-05519		RESISTOR, fxd, 1024K, ±1%, 1/4w
R78	13-04870		RESISTOR, fxd, 6.81K, ±1%, 1/8w
R79	13-04868		RESISTOR, fxd, 2.74K, ±1%, 1/8w
R80	13-04862		RESISTOR, fxd, 1.62K, ±1%, 1/8w
R81	13-02388		RESISTOR, fxd, 2K, ±5%, 1/4w
R82	13-03155		RESISTOR, fxd, 21.5K, ±1%, 1/8w
R83	13-09150-04	TYPE 62 PR (Helitrim)	POTENTIOMETER, 5K, 1 turn
R84	13-09418		RESISTOR, fxd, 24.3K, ±1%, 1/8w
R85	13-04855		RESISTOR, fxd, 9.09K, ±1%, 1/8w
R86	13-09410	TYPE 62 PR (Helitrim)	POTENTIOMETER, 2K, 1 turn
R87	13-04855		RESISTOR, fxd, 9.09K, ±1%, 1/8w
R88	13-0915-07	TYPE 62 PR (Helitrim)	POTENTIOMETER, 2K, 1 turn
R89	13-00365		RESISTOR, fxd, 1K, ±5%, 1/4w
R90	13-00295		RESISTOR, fxd, 330, ±5%, 1/4w
R91	13-01401		RESISTOR, fxd, 750, ±5%, 1/4w
R92	13-03187		RESISTOR, fxd, 820K, ±10%, 1/4w
R93	13-09150-06	TYPE 62 PR (Helitrim)	POTENTIOMETER, 50K, 1 turn

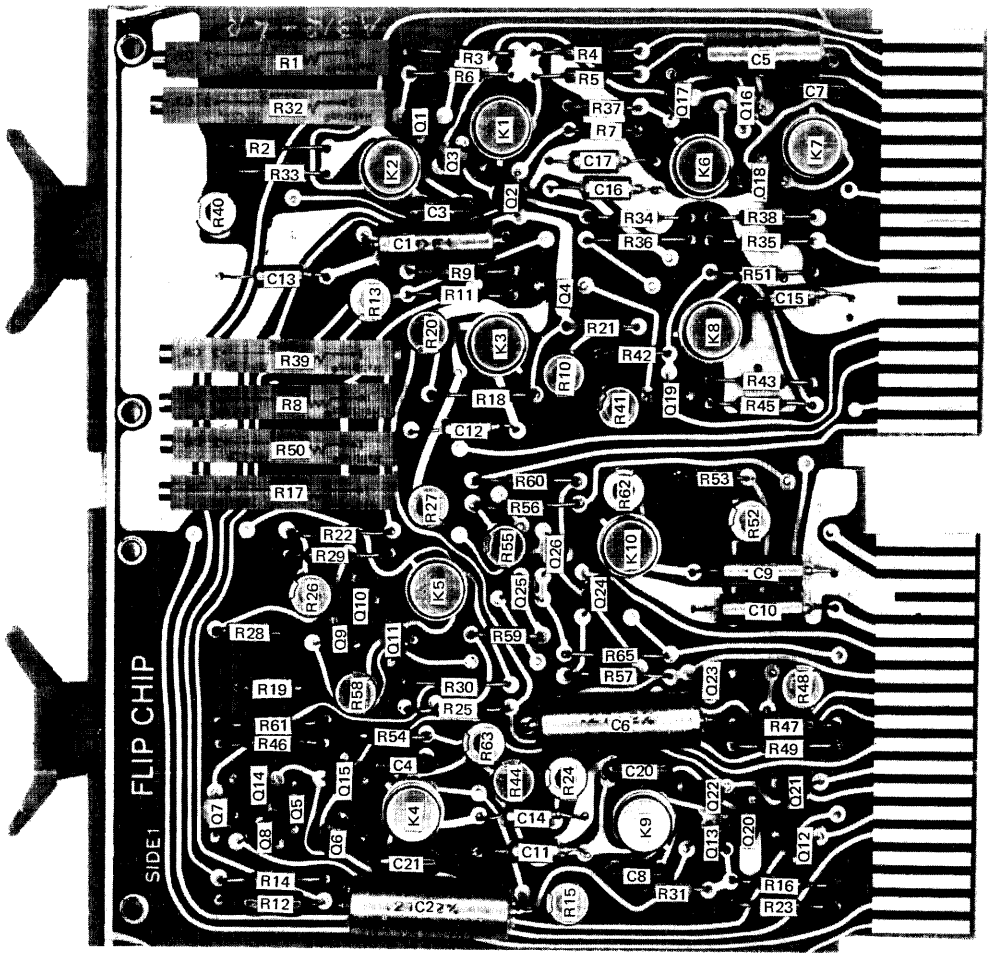


Figure 6-3. Analog Function Generator Module A312, Parts Location Diagram

TABLE 6-4. ANALOG FUNCTION GENERATOR MODULE A312, REPAIR PARTS LIST

Ref Desig	DEC. Stock No.	MFR. Type or Part No.	Description
C1	10-09463		CAPACITOR, 0.47, ±10%
C2	10-09464		CAPACITOR, 0.27, ±2%
C3	10-01739		CAPACITOR, 0.27 pf, 100 wvdc
C4	10-01739		CAPACITOR, 0.27 pf, 100 wvdc
C5	10-09463		CAPACITOR, 0.047, ±10%
C6	10-09464		CAPACITOR, 0.27, ±2%
C7	10-01739		CAPACITOR, 0.27 pf, 100 wvdc
C8	10-01739		CAPACITOR, 0.27 pf, 100 wvdc
C9 and C10	10-04813		CAPACITOR, 10, 20 wvdc
C11 thru C17	10-01776		CAPACITOR, 1, 35 wvdc
C18 and C19	10-00026		CAPACITOR, 680 pfd, 100 wvdc
E1 thru E10	19-09499	LM307	OPERATIONAL AMPLIFIER
Q1	15-09374	2N5459	TRANSISTOR, FET
Q2	15-03409-01	2N6534B	TRANSISTOR
Q3 thru Q6	15-09374	2N5459	TRANSISTOR, FET
Q7	15-03409-01	2N6534B	TRANSISTOR
Q8 thru Q16	15-09374	2N5459	TRANSISTOR, FET
Q17	15-03409-01	2N6534B	TRANSISTOR
Q18 and Q19	15-09374	2N5459	TRANSISTOR, FET
Q20	15-03409-01	2N6534B	TRANSISTOR
Q21 thru Q26	15-09374	2N5459	TRANSISTOR, FET
R1	13-09408	TYPE 78 PR (Helitrim)	POTENTIOMETER, 200, 15 turns
R2	13-02871		RESISTOR, fxd, 1.21K, ± 1%, 1/8w
R3	13-05338	TYPE 78 PR (Helitrim)	POTENTIOMETER, 100K, 15 turns
R4 and R5	13-03312		RESISTOR, fxd, 10K, ±1%, 1/8w
R6	13-03312		RESISTOR, 10K, ± 1%, 1/8w
R7	13-03178		RESISTOR, fxd, 820K, ± 1%, 1/4 w ±10%
R8	13-05338	TYPE 78 PR (Helitrim)	POTENTIOMETER, 100K, 15 turns
R9	13-03312		RESISTOR, fxd, 10K, ± 1%, 1/8w
R10	13-09407	TYPE 62 PR (Helitrim)	POTENTIOMETER, 50K, 1 turn
R11	13-02212		RESISTOR, fxd, 10K, ± 1%, 1/8w
R12	13-09416		RESISTOR, fxd, 31.6K, ± 1%, 1/8w
R13	13-09150-08	TYPE 62 PR	POTENTIOMETER, 500, 1 turn
R14	13-04862		RESISTOR, fxd, 1.62K, ± 1%, 1/8w
R15	13-09150-04	TYPE 62 PR (Helitrim)	POTENTIOMETER, 5K, 1 turn
R16	13-09412		RESISTOR, fxd, 18.2K, ± 1%, 1/8w
R17	13-05338	TYPE 78 PR (Helitrim)	POTENTIOMETER, 100K, 15 turns
R18	13-09413		RESISTOR, fxd, 3.83K, ± 1%, 1/8w
R19	13-03187		RESISTOR, fxd, 820K, ±10%, 1/2w

TABLE 6-4. ANALOG FUNCTION GENERATOR MODULE A312, REPAIR PARTS LIST (cont)

Ref Desig	DEC. Stock No.	MFR. Type or Part No.	Description
R20	13-09159-03	TYPE 62 PR (Helitrim)	POTENTIOMETER, 1K, 1 turn
R21	13-09680		RESISTOR, fxd, 2.7m, ± 10%, 1/4w
R22	13-09419		RESISTOR, fxd, 19.6K, ± 1%, 1/8w
R23	13-09420		RESISTOR, fxd, 8.25K, ± 1%, 1/8w
R24	13-09150-07	TYPE 62 PR (Helitrim)	POTENTIOMETER, 2K, 1 turn
R25	13-09413		RESISTOR, fxd, 9.76K, ± 1%, 1/8w
R26	13-09150-04	TYPE 62 PR (Helitrim)	POTENTIOMETER, 5K, 1 turn
R27	13-09150-06	TYPE 62 PR (Helitrim)	POTENTIOMETER, 50K, 1 turn
R28	13-09680		RESISTOR fxd, 2.7m, ±10%, 1/4w
R29	13-09414		RESISTOR, fxd, 9.76, ± 1%, 1/8w
R30	13-03312		RESISTOR, fxd, 10K, ± 1%, 1/8w
R31	13-09680		RESISTOR, fxd, 2.7m, ± 10%, 1/4w
R32	13-09408	TYPE 78 PR (Helitrim)	POTENTIOMETER, 200, 15 turns
R33	13-02871		RESISTOR, fxd, 1.21K, ± 1%, 1/8w
R34	13-09415		RESISTOR, fxd, 11.5K, ± 1%, 1/8w
R35	13-03312		RESISTOR, fxd, 10K, ± 1%, 1/8w
R36	13-03312		RESISTOR, fxd, 10K, ± 1%, 1/8w
R37	13-03187		RESISTOR, fxd, 820K, ±10%, 1/4w
R38	13-03312		RESISTOR, fxd, 10K, ± 1%, 1/8w
R39	13-05338	TYPE 78 PR (Helitrim)	POTENTIOMETER, 100K, 15 turns
R40	13-09150-40	TYPE 62 PR (Helitrim)	POTENTIOMETER, 5K, 1 turn
R41	13-09150-06	TYPE 62 PR (Helitrim)	POTENTIOMETER, 50K, 1 turn
R42	13-09680		RESISTOR, fxd, 2.7m, ±10%, 1/4w
R43	13-03312		RESISTOR, fxd, 10K, ± 1%, 1/8w
R44	13-09150-04	TYPE 62 PR (Helitrim)	POTENTIOMETER, 5K, 1 turn
R45	13-03312		RESISTOR, fxd, 10K, ± 1%, 1/8w
R46	13-09412		RESISTOR, fxd, 18.2, ± 1%
R47	13-09416		RESISTOR, fxd, 31.6K, ± 1%, 1/8w
R48	13-09150-08	TYPE 62 PR (Helitrim)	POTENTIOMETER, 500, 1 turn
R49	13-04862		RESISTOR, fxd, 1.62K, ± 1%, 1/8w
R50	13-05338	TYPE 78 PR (Helitrim)	POTENTIOMETER, 1K, 15 turns

TABLE 6-5. VOLTAGE REGULATOR MODULE A712, REPAIR PARTS LIST

Ref Desig	DEC. Stock No.	MFR. Type or Part No.	Description
C1	10-00011		CAPACITOR, 47 pf
C2 and C3	10-01776		CAPACITOR, 1, 35V
C4	10-00011		CAPACITOR, 47 pf
C5	10-01776		CAPACITOR, 1, 35V
C6	10-00079		CAPACITOR, 47 pf
C7 thru C10	10-04815		CAPACITOR, 100
C11 and C12	10-01610		CAPACITOR, 0.01
D1	11-03441	1N756A	SILICON DIODE, ZENER DIODE, 1N756A
D2	11-03016	MOTOROLA MDA 942-3	SILICON DIODE BRIDGE
E1 and E2	19-09371	LM 300	REGULATOR
H1 and H2	12-02313		HEAT SINK, THERMALLOY, #2211B
Q1	11-03016	2N4036	TRANSISTOR
Q2	15-02979	2N3638B	TRANSISTOR
Q3	15-09391	2N2270	TRANSISTOR
Q4	15-02937	2N3568	TRANSISTOR
R1	13-09421		RESISTOR, 2,± 5%, ½w
R2	13-02941		RESISTOR, fxd, 14.7K, ± 1%, 1/8w
R3	13-03303		RESISTOR, fxd, 2.61K, ± 1%, 1/8w
R4	13-02941		RESISTOR, fxd, 14.7K, ± 1%, 1/8w
R5	13-03303		RESISTOR, fxd, 2.61K, ± 1%, 1/8w
R6	13-09422		RESISTOR, fxd, 5.1
R7	13-00229		RESISTOR, fxd, 100
R8	13-00391		RESISTOR, fxd, 1.5K
R9	13-00229		RESISTOR, fxd, 100

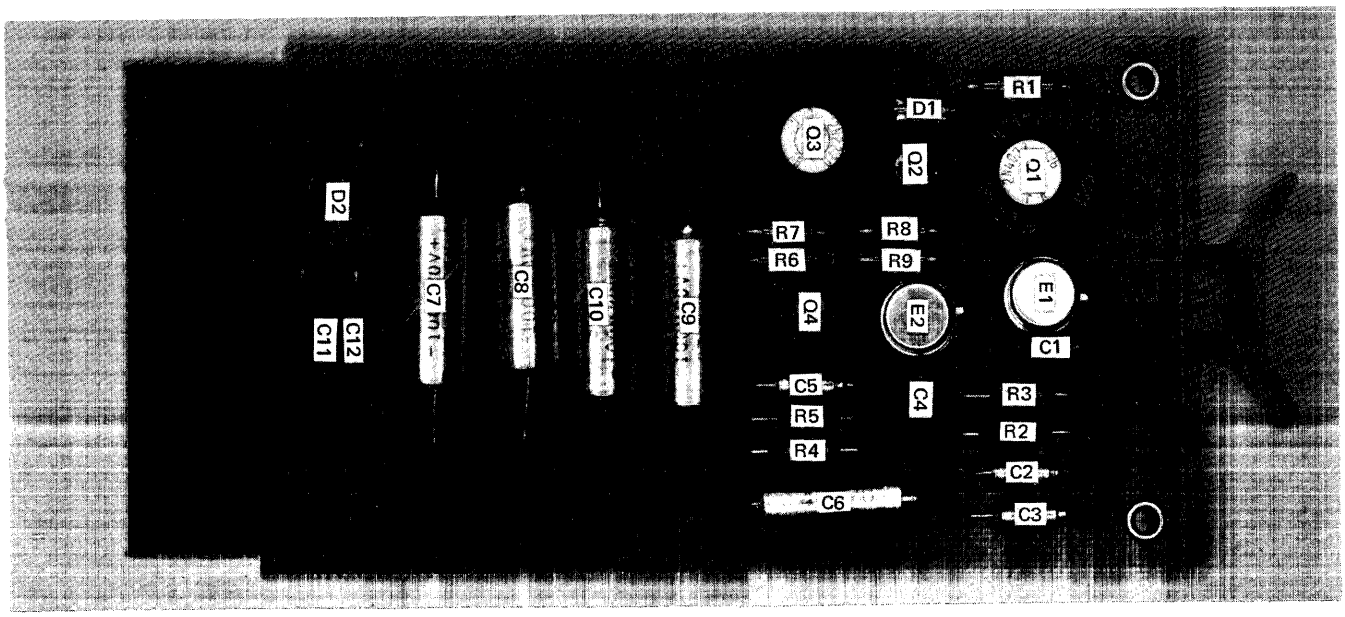


Figure 6-4. Voltage Regulator Module, Parts Location Diagram

CHAPTER 7
DIAGRAMS

This chapter contains general reference diagrams that will aid in maintenance and repair of the KV controller. Table 7-1 is a list of the diagrams contained in this chapter.

TABLE 7-1. LIST OF DIAGRAMS

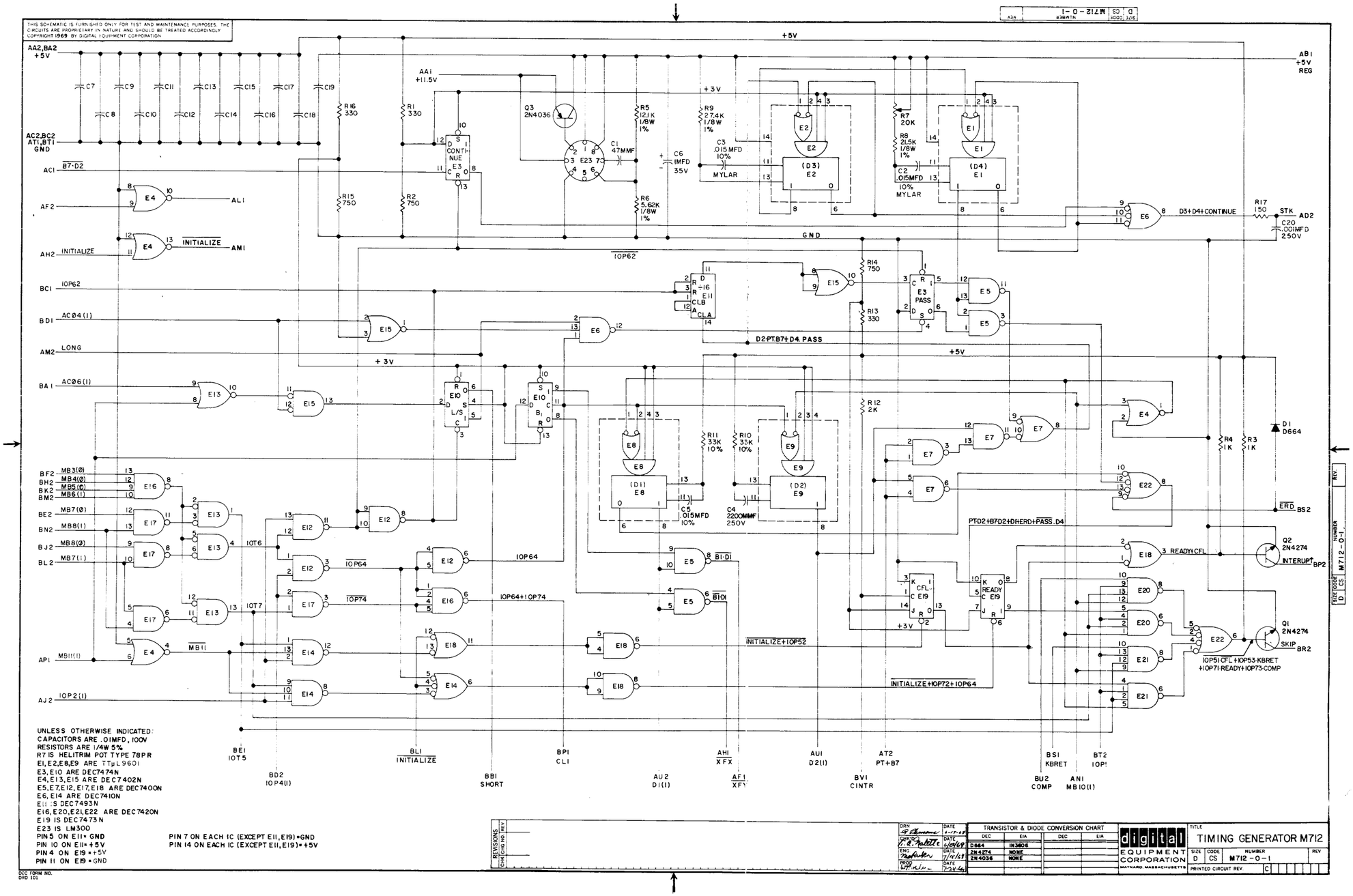


Figure 7-1. Timing Generator Module M712, Schematic Diagram, M712-0-1

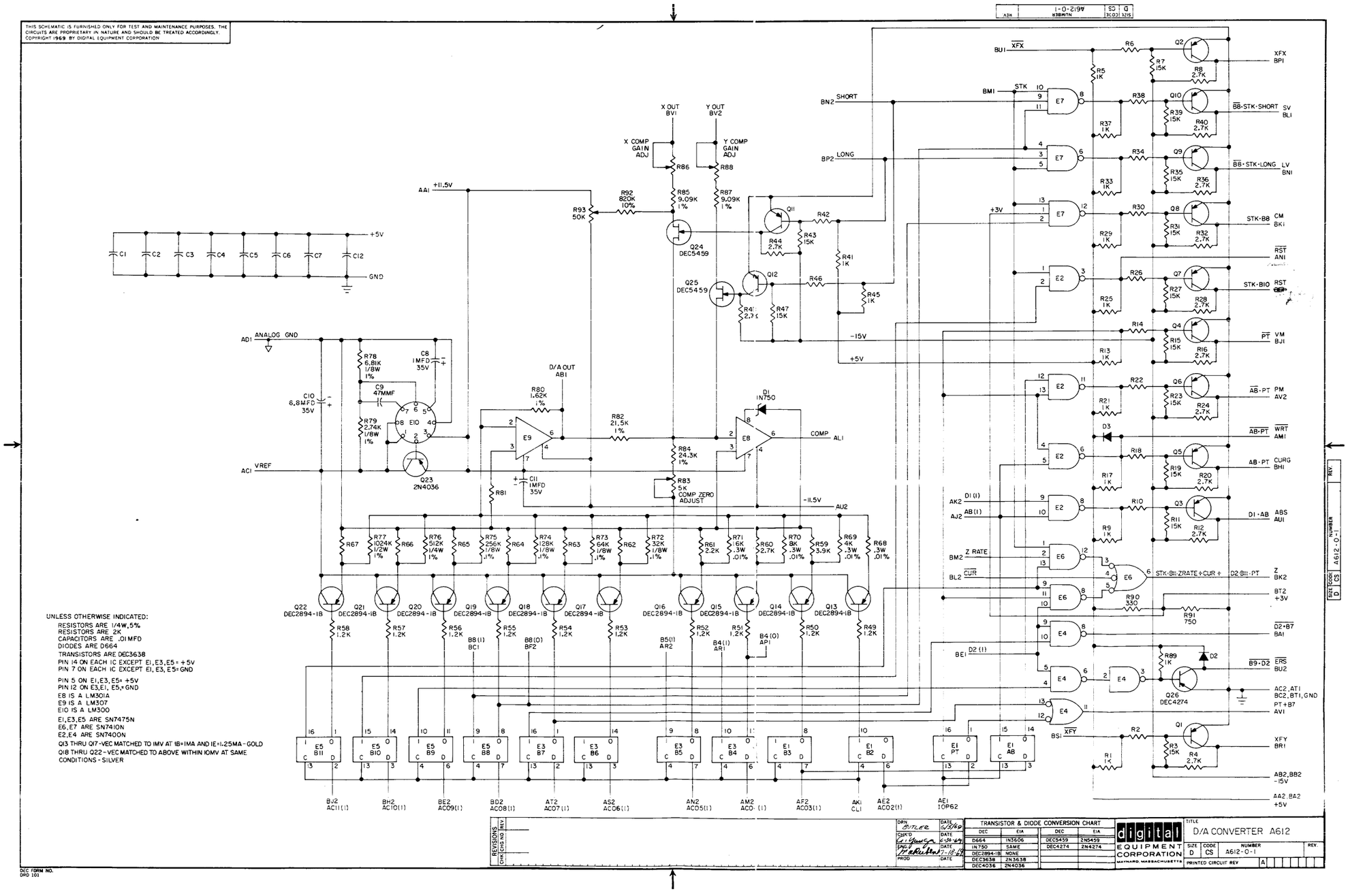


Figure 7-2. Digital-to-Analog Converter and Gate Logic Module A612, Schematic Diagram, A612-0-1

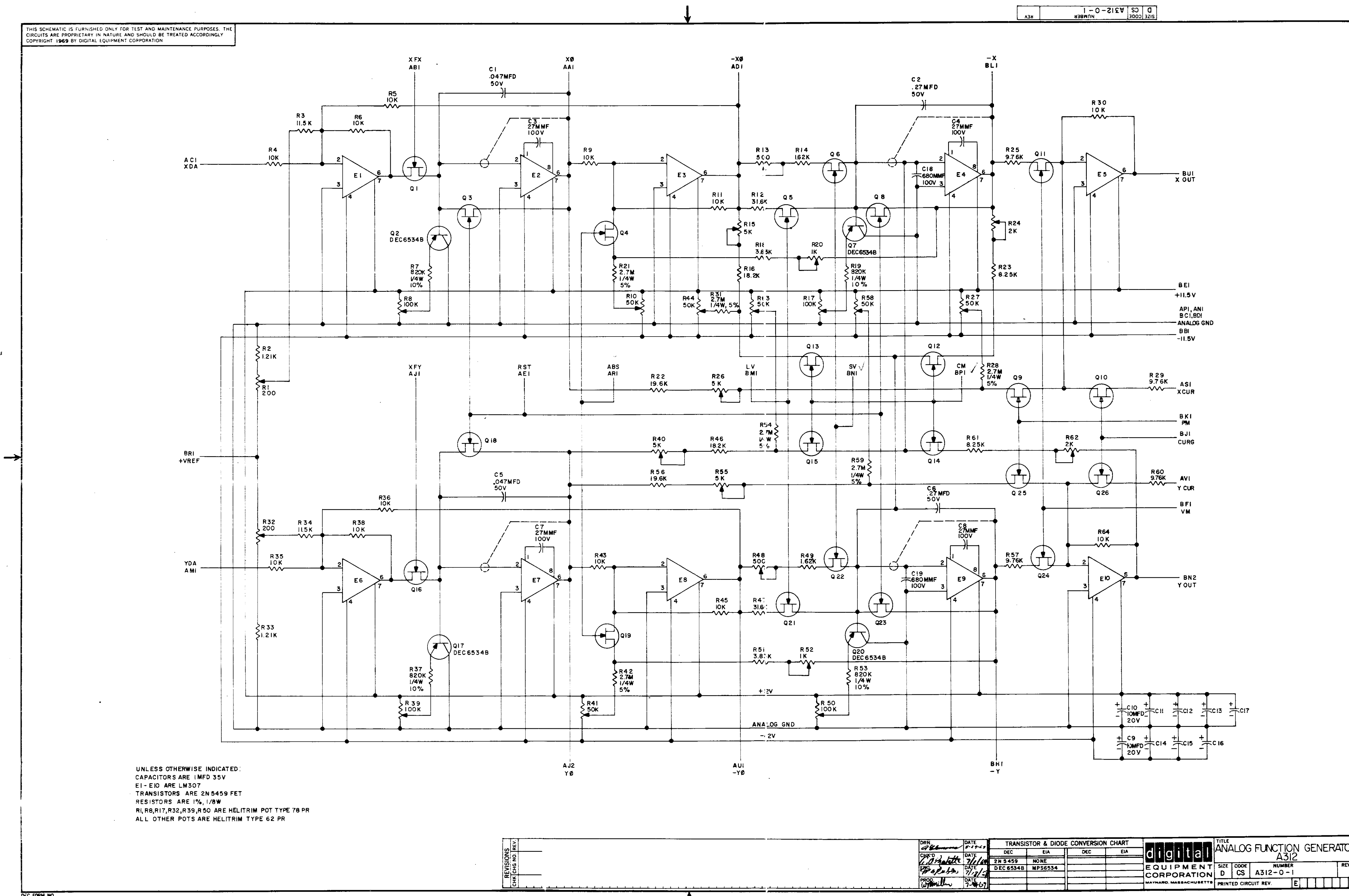


Figure 7-3. Analog Function Generator Module A312, Schematic Diagram, A312-0-1

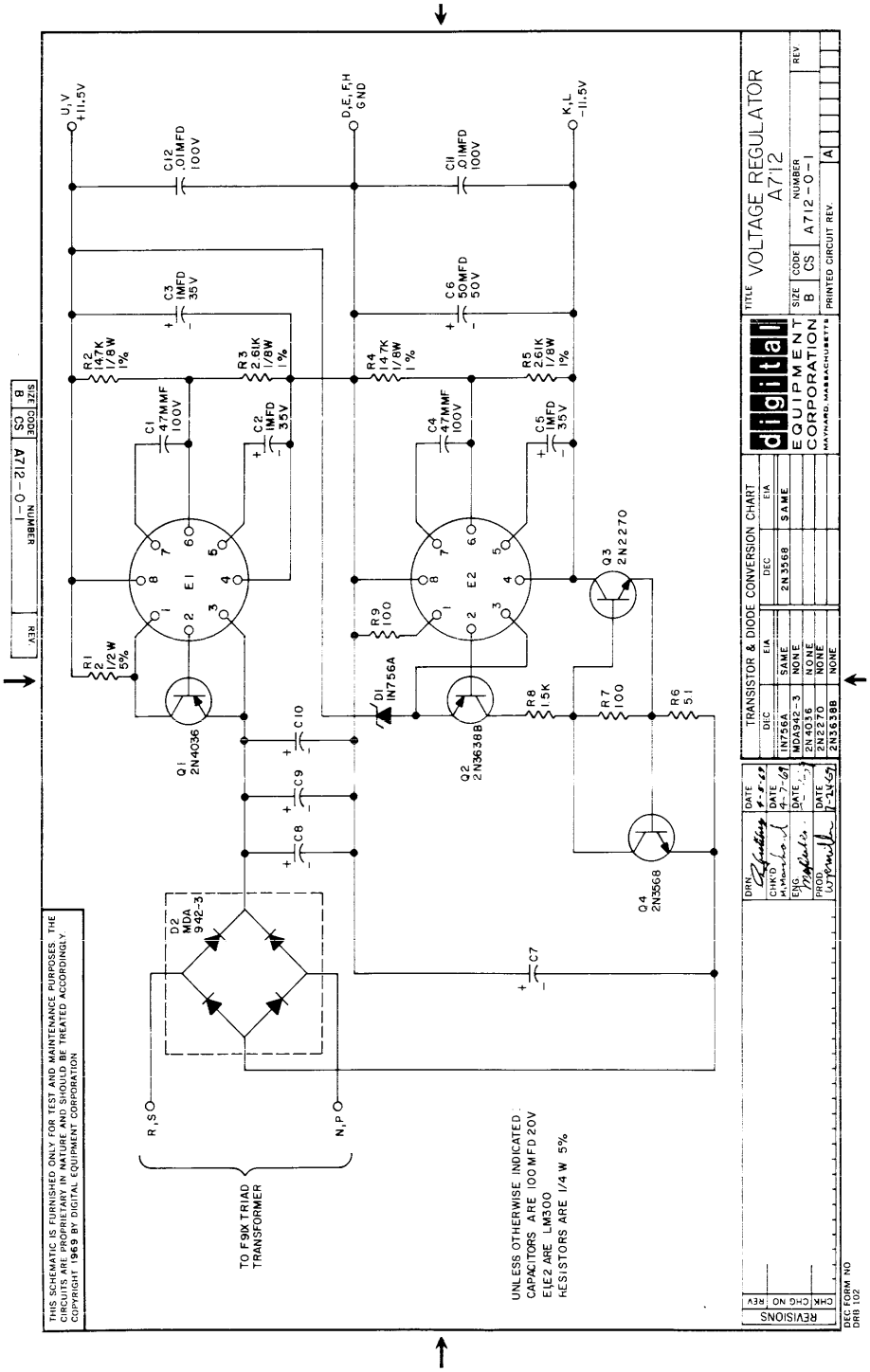


Figure 7-4. Voltage Regulator Module A712, Schematic Diagram, A712-0-1

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
+12V	H21U2	J25E1		#24 WIRE
"	H21U2	H24A1		"
"	H21V2	H23A1		"
"	H21V2	J21D1		(#30 WIRE)
-12V	H21K2	J25B1		#24 WIRE
"	H21K2	H24U2		"
"	H21L2	J21V2		(#30 WIRE)
ANALOG GND	H21C2	H21D2		SOLID BUS STRAP
	H21D2	H21E2		"
	H21E2	H21F2		"
	H21F2	H21H2		"
	H21E2	J25C1		#24 WIRE
	J25C1	J25D1		SOLID BUS
	H21E2	H24D1		#24 WIRE
VREF	H24C1	J25R1		
AC INPUT	H21N2	AC SECONDARY	GREEN	FROM TRIAX F91X
AC INPUT	H21F2	AC SECONDARY	YELLOW	MOUNTED AT END OF
AC INPUT	H21R2	AC SECONDARY	RED	FANS
AC INPUT	FAN PWR AC	AC PRIMARY	BLK/WHT	"
AC INPUT	FAN PWR AC	AC PRIMARY	BLK/RED	"

REVISIONS			
REV.	DATE	CHG. NO.	APP'D.
ORIG.	2/24/69	8I-00036	A.M.
A	6/2/69	8I-00056	

DRN. Betty Vadnais	DATE 2-24-69	
CHK'D.	DATE 2-27-69	
ENG.	DATE 3/3/69	
PROJ. ENG.	DATE 3/3/69	
PROD.	DATE 3-3-69	
FIRST USED ON		
SCALE		
SHEET OF		

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE
GENERAL WIRING SHEET
FOR
KV8/I MODIFICATION

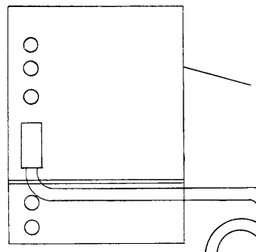
SIZE	CODE	NUMBER	REV.
A	WL	KV8I-0-1	A

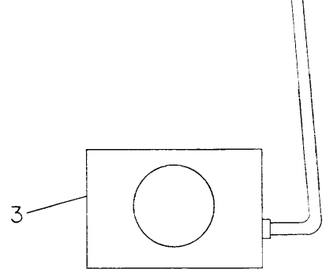
DIST.

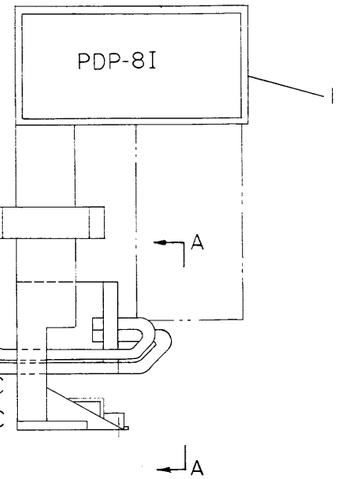
DEC FORM NO.
DRA 104

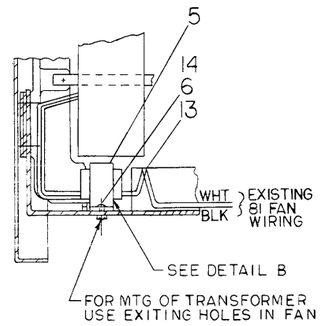
Figure 7-5. General Wiring Sheet for KV8I Modification, KV8I-0-1

NOTES
1 DO NOT CUT TRANSFORMER LEADS NOT USED. TAPE ENDS

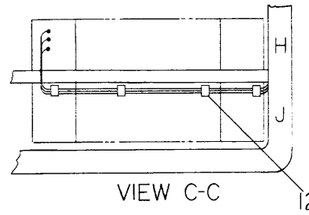




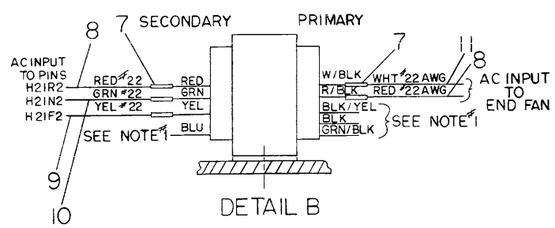




SECTION A-A



VIEW C-C



DETAIL B

FIRST USED ON OPT/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
KV8I		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH

DRN.	W. Crabbe	DATE 2/5/69
CHK'D.	E.W. Ross	DATE 4/16/69
ENG.	[illegible]	DATE 5/13/69
PROJ. ENG.	[illegible]	DATE 5/13/69
PROD.	W. Mueller	DATE 6-1-69

FIRST USED ON
SCALE NONE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE
KV8I
DISPLAY CONTROL

SIZE D | CODE UA | NUMBER KV8I-0-0 | REV.
DIST.

REVISIONS | REV. | CHANGE NO. | CHK

DEC FORM NO. DRD 100

Figure 7-6. KV8I Display Control, KV8I-0-0

REVISIONS	REV	CHANGE NO	CHK

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
KV8I		PARTS LIST		

UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN	Kay Hay	DATE 3-7-69
CHK'D		DATE
ENG.		DATE
PROJ. ENG.		DATE
PROD.		DATE

NEXT HIGHER ASSY: D-UA-KV8I-Ø-Ø

SCALE

SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: KV8I CONTROL LOGIC

SIZE	CODE	NUMBER	REV.
D	BS	KV8I-Ø-2	

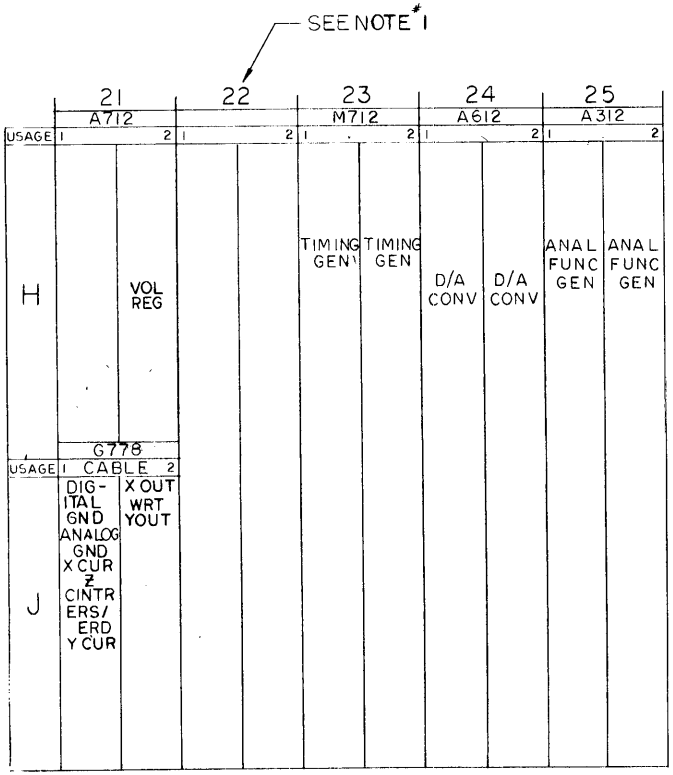
DIST.

DEC FORM NO. DRD 102A

Figure 7-7. KV8I Control Logic, KV8I-0-2

NOTES

1. SLOT HJ22 RESERVED FOR KV OPTION



FIRST USED ON OPT/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
KV81		PARTS LIST		

UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY ✓
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —

FINISH —

DRN. W.K. Gabbe	DATE 4/2/69	
CHK'D. F.W. Ross	DATE 4/17/69	
ENG. Martucci	DATE 5/23/69	
PROJ. ENG. M. Gulczynski	DATE 5/23/69	
PROD. W.P. Miller	DATE 6-1-69	

NEXT HIGHER ASSY
A-ML-KV8I-O

SCALE —

SHEET 1 OF 1

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE
MODULE UTILIZATION KV8I

SIZE	CODE	NUMBER	REV.
C	MU	KV8I-Ø-3	

DIST.

REVISIONS | REV. | CHANGE NO. | CHK

DEC FORM NO. DRC 100

Figure 7-8. Module Utilization KV8I, KV8I-0-3

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
$\overline{\text{K7 . D2}}$	H23C1	J24A1		
$\overline{\text{XFX}}$	H23F1	J24S1		
$\overline{\text{XFX}}$	H23H1	J24U1		
IOP 1(1) 1	J33F2	J23T2		
$\overline{\text{INIT}}$	H23M1	J23L1		
D2(1)	H23U1	J24E1		
D1(1)	H23U2	H24K2		
PT + B7	H23T2	H24V1		
LONG	H23M2	J24P2		
STK	H23D2	J24M1		
AC06(1)	J23A1	H24S2		
SHORT	J23B1	J24N2		
AC04(1)	J23D1	H24M2		
IOP62	J23C1	H24E1		
CL1	J23P1	H24K1		
$\overline{\text{ERD/ERS}}$	J24U2	J21S2		
$\overline{\text{ERD/ERS}}$	J23S2	J24U2		
COMP	J23U2	H24L1		
Z	J24K2	J21K2		
$\overline{\text{WRT}}$	H24M1	J21M1		
CUR INTR	J23V1	J21M2		
K BRET	J23S1	J23C2		
DIGITAL GND	H21H2	J21D2		
ANALOG GND	H21F2	J21E2		
$\overline{\text{CUR}}$	H24M1	J24L2		
YD/A	H24B1	H25M1		

REVISIONS			
REV.	DATE	CHG. NO.	APP'D.

DRN. K. RUSS	DATE 4/8/69	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. K. RUSS	DATE 4/8/69	
ENG.	DATE	TITLE GENERAL WIRING SHEET
PROJ. ENG.	DATE	FOR KV8I
PROD. W.P. Mills	DATE 6-1-69	
FIRST USED ON #		
SCALE #		SIZE A | CODE WL | NUMBER KV8I-0-5 | REV.
SHEET 1 OF 3		DIST.

DEC FORM NO. DRA 104

Figure 7-9. General Wiring Sheet for KV8I, KV8I-0-5 (Sheet 1)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
XD/A	H25M1	H25C1		
ABS	H24U1	H25R1		
CURG	J24H1	J25J1		
VM	J24J1	J25F1		
PM	H24V2	J25K1		
SV	J24L1	J25N1		
LV	J24N1	J25M1		
XFX	J24P1	H25B1		
XFY	J24R1	H25J1		
CM	J24K1	J25P1		
RST	J24F1	H25E1		
Z RATE	J24M2	J24T2		
X OUT	J24V1	J25U1		
X,OUT	J25U1	J21B1		
Y OUT	J24V2	J25N2		
Y OUT	J25N2	J21P1		
X CUR	H25S1	J21H2		
Y CUR	H25V1	J21T2		
+3V	D1ØE2	EØ9M1		REMOVE IF PRESENT
	EØ9V1	EØ9L2		
	EØ9L2	EØ9M1		
	EØ9M1	EØ9P1		
+3V	EØ9P1	EØ9P2		
IOP 1 (Ø)	EØ9M2	E19R2		M113 REQ'D IN EØ9
IOP 2 (Ø)	EØ9R1	E19U1		IF NOT PRESENT
IOP 4 (Ø)	EØ9R2	E19V1		

REVISIONS			
REV.	DATE	CHG. NO.	APP'D.

DRN. K.RUSS	DATE 4/8/69	
CHK'D. K. RUSS	DATE 4/8/69	
ENG.	DATE	
PROJ. ENG.	DATE	
PROD.	DATE 6/6/69	
FIRST USED ON #		
SCALE #		
SHEET 2 OF 3		

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE
GENERAL WIRING SHEET
FOR
KV8I

SIZE	CODE	NUMBER	REV.
A	WL	KV8I-Ø-5	

DIST.

DEC FORM NO.
DRA 104

Figure 7-9. General Wiring Sheet for KV8I, KV8I-0-5 (Sheet 2)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
IOP 1 (1) 1	EØ9N2	J33F2		
IOP 2 (1) 1	EØ9S1	J33H2		
IOP 4 (1) 1	EØ9S2	J33F1		

REVISIONS			
REV.	DATE	CHG. NO.	APP'D.

DRN. K. RUSS	DATE 4/8/69	
CHK'D. K. RUSS	DATE 4/8/69	
ENG.	DATE	
PROJ. ENG.	DATE	
PROD.	DATE 6-1-69	
FIRST USED ON #		
SCALE #		
SHEET 3 OF 3		

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE
GENERAL WIRING SHEET
FOR
KV8I

SIZE	CODE	NUMBER	REV.
A	WL	KV8I-Ø-5	

DIST.

DEC FORM NO. DRA 104

Figure 7-9. General Wiring Sheet for KV8I, KV8I-0-5 (Sheet 3)

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE 5/15/69

TITLE KV8/I Display Acceptance Procedure

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A		00001	--------	-----	a E.D.	8/8/69

ENG	APPD	SIZE	CODE	NUMBER	REV
		A	SP	KV8I-0-6	A

DEC FORM NO.
DRA 107

SHEET 1 OF 3

Figure 7-10. KV8I Display Acceptance Procedure, KV8I-0-6 (Sheet 1)

ENGINEERING SPECIFICATION digital **CONTINUATION SHEET**

TITLE

Scope: to define the procedure to accept a KV8/I system for shipment.

Test Hardware:

1) PDP8/I computer wired for KV8/I option and with Teletype.
2) KV8/I display option modules (M712, A612, A312, A712).
3) VT01 Storage Display Unit (modified Tektronix 611).
4) H306 Joystick Control.
5) Display system, dual cable.

Test Software:

KV8/I Display Diagnostic - binary tape, Maindec-8/I-DC6A-PB(L), writeup, 8/I-DC6B-D(D), and listing.

Procedure:

1) Perform Q C inspection.
2) Check KV8/I and VT01 alignment using diagnostic (Sec. 5.3.1. thru 5.3.3), and touchup where required. Patterns must meet the performance specs given in performance specs for KV8/I controller writeup.
3) Run the main diagnostic (Sec. 5.3.5.1, S/A200) for ten minutes.
4) Run the cursor diagnostic (Sec. 5.3.5.2) for approximately 20 interrupts.

	SIZE	CODE	NUMBER	REV
	A	SP	KV8I-0-6	A

DEC FORM NO DRA 108

SHEET 2 OF 3

Figure 7-10. KV8I Display Acceptance Procedure, KV8I-0-6 (Sheet 2)

5) Unit is accepted when steps 2 thru 4 can be successfully completed and performance specs for KV8/I controller writeup, is met. Error halts greater than 500 is step 2 can be corrected by suitable realignment performed in step 1.

. Shipping Hardware:

1) PDP8/I computer wired for KV8/I with Triad F91X transformer. PDP8/I may or may not be already installed.
2) KV8/I display option (modules M712, A612, A312, A712).
3) VT01 Storage Display Unit in special shipping container.
4) H306 Joystick Control.
5) 20 ft. display system dual cable.

Shipping Software:

1) KV8I Display System Software Package
2) KV Maintenance Manual.
3) Tektronix 611 Manual.
4) Complete set of prints.

Figure 7-10. KV8I Display Acceptance Procedure, KV8I-0-6 (Sheet 3)

DIGITAL EQUIPMENT CORPORATION

MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE 5/15/69

TITLE Performance Specifications for KV8/I Controller and VT01 Display

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

ENG	APPD	SIZE	CODE	NUMBER	REV
[illegible]	[illegible]	A	SP	KV[illegible]-0-7	

DEC FORM NO.
DRA 107

SHEET 1 OF 10

Figure 7-11. Performance Specifications for KV8I Controller and VT01 Display, KV8I-0-7 (Sheet 1)

I. Line Drawing Capability (1),(2) - Controller.

A. Scope - The KV8/I controller shall be capable of drawing linear vectors, circular vectors, or point plotting.

A.1.1. Linear vectors shall be drawn using a stroke method. Such vectors may either be addressed in absolute mode, giving the x,y coordinates of the end point of the vector, or in relative mode, giving $\Delta x, \Delta y$ coordinates of the end point of the vector relative to the present location.

A.1.2. Maximum length of any stored vector should not exceed 8" to guarantee storage.

A.1.3. Linear absolute vectors shall close within .02" for vectors up to 6".

A.1.3.1 There is no guaranteed closure for linear relative vectors.

A.1.4. Linear vectors may be executed at two execution rates, short vector 275 us $\pm$ 10 us or long vector (4.08 ms).

---

(1) All performance specifications stated herein are only valid after the KV controller has been aligned according to the procedures outlined in the KV diagnostic write up (Maindec-8I-D6CA)

(2) All performance specifications as given are only valid for the temperature at which the system was initially aligned, except where stated otherwise. See Section VI of this writeup.

Figure 7-11. Performance Specifications for KV8I Controller and VT01 Display, KV8I-0-7 (Sheet 2)

A.1.4.1. A long vector execution is required if the vector length exceeds 3/8". A long vector execution of less than 3/8" will cause deterioration in line quality (excess line width and lower resolution).

A.1.4.2. A short vector execution exceeding 3/8" length violates the storage capability of the VT01 and the accuracy of the KV controller. Short vectors of less than 3/8" will meet all accuracy specifications stated herein.

A.2.1. Circular arc vectors shall be drawn by a stroke method. Such vectors are addressed by giving the x,y coordinates of the center of a circular arc. The present location of the integrators (which may be established by an invisible absolute linear vector) defines the starting location of the arc and hence a point on the circumference.

A.2.2. Maximum radius of a stored arc vector should not exceed 3" to guarantee storage.

A.2.3.1 Circular arc vectors up to 6 inches diameter shall close within .02 inches radially and within .02 inches circumferentially.

A.2.3.2 Circular arc vectors shall center (rotate about) the selected screen location within an accuracy of .02 in. (A zero radius circle may just begin to show an open center).

Figure 7-11. Performance Specifications for KV8I Controller and VT01 Display, KV8I-0-7 (Sheet 3)

A.2.4 Circularity of circular vectors shall be ± 5% (i.e. semi-major and semi-minor axis not to differ by more than ± 5%).

A.2.5.1 Circular arc vectors shall be $90^{\circ} \pm 1^{\circ}$ for long vector execution or $5.625^{\circ} \pm .07^{\circ}$ for short vector execution.

A.2.5.2 Circular arc vectors shall rotate at a radian rate of $.1^{0}$ per 4.5 us adjustable ± 10%.

A.2.5.3 All circular vectors rotate clockwise from their starting location about the selected center.

A.3.1 Point plot mode shall store a dot addressed as X,Y.

A.3.2 Maximum point plot range is ± 12" about origin (+511 to -512 decimal coordinates).

A.3.3. Point plot shall position within .02" of an address referenced by a long linear absolute vector.

B. The KV controller shall provide a hardware reset function.

B.1 Reset will position a subsequent point plot or linear vector to within .04" of the true origin (i.e. a Ø,Ø absolute linear vector) when executed from a position not to exceed 6" from the origin using long vector execution.

B.2 Reset shall recover from a latch-up condition (integrators or sample-holds saturated at power supply potential) in less than .5 seconds, when issued as

Figure 7-11. Performance Specifications for KV8I Controller and VT01 Display, KV8I-0-7 (Sheet 4)

reset-continue.

C. The KV controller shall provide a vector-continue function.

C.1 The vector continue permits disabling of the hardware timer allowing auxilliary timing of the reset and circular arc vectors.

C.2 Reset continue shall be permitted in cursor display mode.

II. Line Drawing Capability - VTØ1 Display

A. Line Quality

A.1.1 The VTØ1 shall provide a resolution of at least 300 stored line pairs in point plot mode (line width of .01 inches)measured along the X or Y axis.

A.1.2 The VTØ1 shall provide a resolution of at least 150 stored line pairs in linear vector mode (.02 in line width) measured along the X or Y axis.

A.2 Maximum variation in line width shall not exceed 3:1 over the quality area of the scope (6" by 7 1/2") for long or short vectors executed under the definition of Par. A.1.4.

A.3 Line straightness deviation from the mean shall not exceed ± .5% of line length.

A.4 Line continuity: dropout shall not exceed .01" per dropout for each dropout area.

Figure 7-11. Performance Specifications for KV8I Controller and VT01 Display, KV8I-0-7 (Sheet 5)

A.5 Line smoothness: noise and wiggle amplitude not to exceed ± .015"

B. VTØ1 Cursor

B.1 Cursor intensity shall be at least 2 ft. lamberts without causing storage of the cursor within the quality area.

C. Warmup and Stabilization

C.1 The VTØ1 shall require a maximum of 30 minutes warmup to provide stable cursor write-thru and vector storage properties.

D. All other VTØ1 specs are given in the Tektronix 611 manual except where such specs conflict with those given here.

III. Scope Control Functions

A. The KV controller shall provide means for programmed erasure of the VTØ1 display with hardware lockout of the ready flag performed by the VTØ1.

B. The KV controller shall provide means to activate and display the VTØ1 write-thru cursor. Such cursor will appear as an ellipse of approximately .1" major axis and will respond to the application of ± .5 volt analog signals to the external cursor input terminals of the controller, producing full screen deflection of the cursor.

C. The controller shall provide for programmed control of the Z axis (intensify) function of the VTØ1.

Figure 7-11. Performance Specifications for KV8I Controller and VT01 Display, KV8I-0-7 (Sheet 6)

IV. Timing Functions

A. The KV control shall provide two hardware timing functions - long (~4 ms) and short (~.25 ms).

B. The KV control provides a delay of 100 us ± 30 us to allow input data to settle.

C. Drift Rates.

C.1 The input (sample-hold) registers shall not drift greater than ± 30 coordinates (.36" for pt plot) per second. (This means the maximum permitted time between the load data and execute commands should not exceed 15 ms).

C.2 The output (integrator) registers shall not drift greater than ± 6 coordinates (.072" in vector mode) per second. (This means absolute vectors should be executed at least 10 vectors per second, and relative vectors should be executed at the full speed rates of Par. D. below).

D. Vector Execution Rates

D.1 Linear vectors may be executed up to 1750 short vectors/sec. or 225 long vectors/sec.

D.2 Points may be executed up to 3000 pts./sec.

D.3 Circles require 16.2 ms per circle, or an angular rate of .1 degree per 4.5 us. This time if invariant (i.e. all circles are executed

Figure 7-11. Performance Specifications for KV8I Controller and VT01 Display, KV8I-0-7 (Sheet 7)

at the same angular rate).

V. D/A and A/D Facilities

A. The controller shall contain a 10 bit digital to analog converter producing 0 to -4 volts ± 5% for a Ø777 to 1ØØØ two's complement input range (ØØØØ produces -2 volts nominally). The reference for this D/A shall be internally supplied and shall be 2.45 volts ± .1 volts.

B. The KV controller shall provide an analog comparator and suitable switching paths to measure any of six analog sources (X or Y sample-hold, X or Y integrators, and X or Y external (cursor) input). This comparator shall provide an accuracy of at least 1% (± 4 digital counts) of the true input, when used with a successive approximation A to D conversion subroutine program.

B.1 The external (cursor) inputs shall accept ± 1 volt ± 10% input signals to provide the full +511 to -512 coordinate range.

B.2 The comparator shall require at least 50 us per successive approximation step (or approximately 1 ms to make a complete 10 bit reading) to permit the comparator to settle to the accuracy stated above.

Figure 7-11. Performance Specifications for KV8I Controller and VT01 Display, KV8I-0-7 (Sheet 8)

VI. Environmental

A. Maximum permitted operating temperature range 10°C to 40°C.

B. Maximum temperature deviation before readjustment of system may be required ± 3°C (± 5°F) about temperature when initially calibrated.

C. Maximum humidity not to exceed 70% to meet above specs.

D. Controller cannot tolerate shock or vibration since the alignment is likely to change.

VII. Power Supply

A. A 712 power supply requires an input of 28 volts CT AC ±2.8 Volts @ 47 to 63 H_Z. This is normally supplied by a TRIAD F91X/transformer mounted to receive power off the fan power bus of the computer.

B. The A712 supplies +11.5V ±1V @ 100 ma and -11.5 ±1V @ 100 ma with ripple not to exceed 50 mv.

C. It is preferred to use KV8/I graphic system on AC power lines free of inductive loads.

D. Total dissipation of the KV controller is less than 5 watts.

E. The KV controller requires + 5V @ 395 ma and - 15V @ 37 ma supplies in addition to the AC supply above.

VIII. Physical

A. The basic controller consists of 4 Flip Chip Modules:

A712 - Power Supply: Standard size Flip Chip module

Figure 7-11. Performance Specifications for KV8I Controller and VT01 Display, KV8I-0-7 (Sheet 9)

M712 - Timing Generator - Double height standard size Flip Chip module.

M612 - D/A Converter - Double height standard size Flip Chip module.

A312 - Analog Function Generator - Double height standard size Flip Chip module.

In the PDP 8/I, these modules occupy the following locations:

H21	A712
HJ23	M712
HJ24	A612
HJ25	A312

B. The KV8/I requires a special cable connector type G778 which occupies slot J21.

C. The KV controller in addition requires a TRIAD F91X, trans. mounted next to the fan housing.

Figure 7-11. Performance Specifications for KV8I Controller and VT01 Display, KV8I-0-7 (Sheet 10)

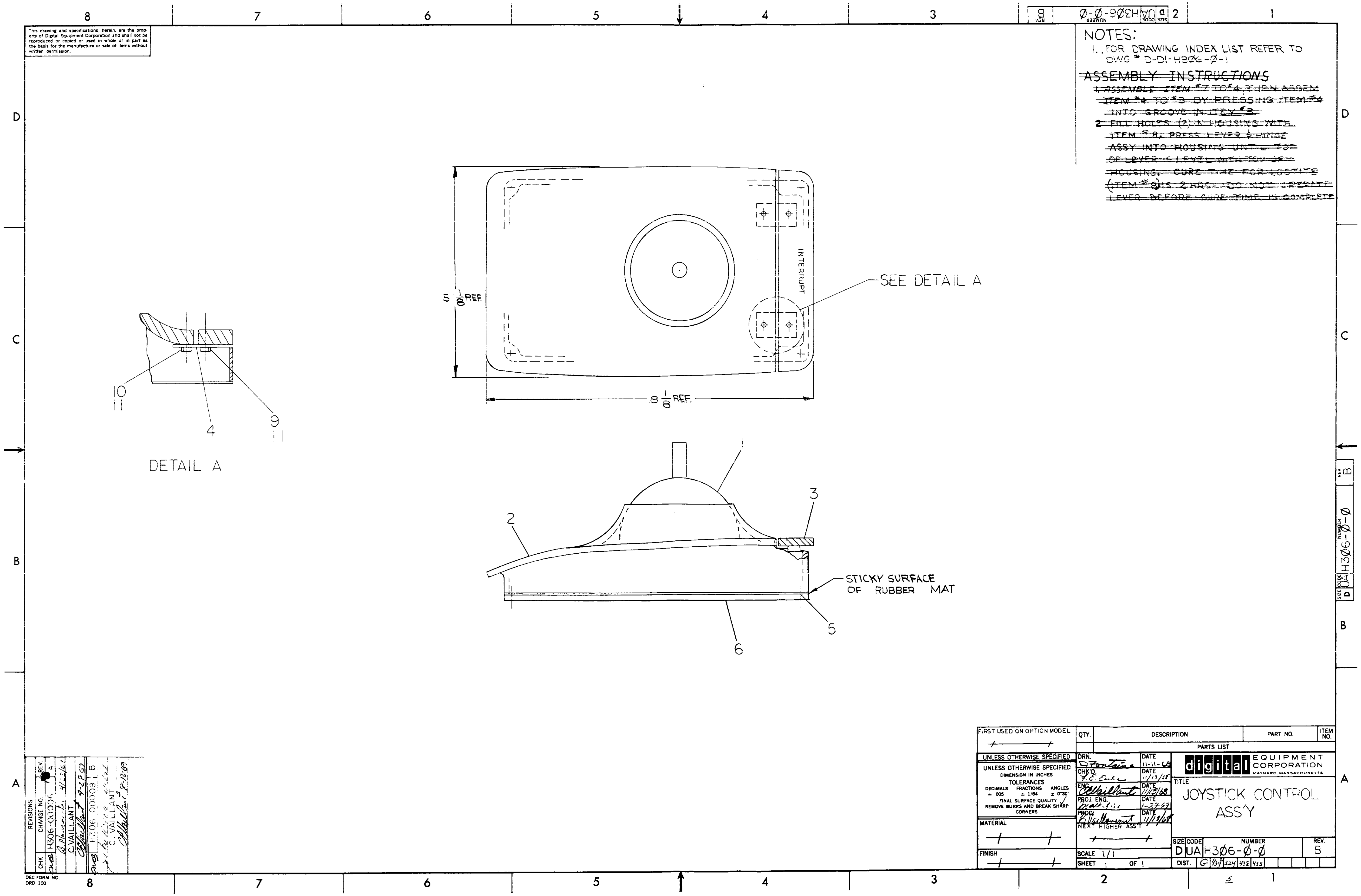


Figure 7-12. Joystick Control Assembly, H306-0-0

Digital Equipment Corporation
Maynard, Massachusetts

digital

printed in U.S.A.